

LFAA SIGNAL PROCESSING SYSTEM DETAILED DESIGN DOCUMENT

Document number SKA-TEL-LFAA-0500035
Context ..... DRE
Revision 01
Author ..... W. Turner
Date 2018-11-01
Document Classification ..... FOR PROJECT USE ONLY
Status ..... Released

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			Date:	Nov 7, 2018

DOCUMENT HISTORY

Revision	Date of Issue	Engineering Change Number	Comments
01	2018-11-01	-	First Release

DOCUMENT SOFTWARE

	Package	Version	Filename
Wordprocessor	MsWord	Word 2016	SKA-TEL-LFAA-0500035_LFAA Signal Processing System DDD Report_20181025.docx
Block diagrams			
Other			

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LIST OF ABBREVIATIONS

AAn ..... Array Assembly phase n
AADC..... Aperture Array Design and construction Consortium
AAVS ..... Aperture Array Verification System
AC..... Alternate Current
AD ..... Analogue to Digital
ADC ..... Analogue to Digital converter
AD-n ..... nth document in the list of Applicable Documents
ADD..... Architecture Design Document
ADU..... Analogue to Digital Unit
AIV ..... Assembly Integration and Verification
API.....Application Programming Interface
APIU ..... Antenna Power Interface Unit
ARM ..... Advanced RISC Machine
ATE..... Automatic Test Equipment
AXI4..... Advanced eXtensible Interface 4
BOM..... Bill Of Material
C2C..... Chip to Chip
CBF..... Central Beamformer
CCB..... Configuration Control Board
CDR ..... Critical Design Review
CI..... Configuration Item
CISPR..... Comité Internationale Speciale des Perturbations Radioelectriques
COTS ..... Commercial Off the Shelf
CPF..... Central Processing Facility
CPLD..... Complex Programmable Logic Device
CM ..... Configuration Manager
CMB ..... Cabinet Management Board
CPU ..... Central Processing Unit
CSP..... Central Signal Processor
DAQ..... Data Acquisition
dBm..... decibel to 1 mW power
dBFS ..... decibel to full scale
DC ..... Direct Current
DDBH ..... Digital Data Back Haul
DDD..... Detailed Design Document
DDR..... Double Data Rate (Memory)
DHCP..... Dynamic Host Configuration Protocol
DPLL ..... Digital Phase Locked Loop
DRP ..... Dynamic Reconfiguration Port
DSP..... Digital Signal Processing
DUT ..... Device Under Test
DWDM ..... Wavelength Multiplexing
ECP..... Engineering Change Proposal
EDA ..... Engineering Data Archival (in TM)
EICD ..... External Interface Control Document
EMC ..... Electro Magnetic Compatibility
EMI..... Electro Magnetic Interference
ENOB..... Equivalent Number of Bits
ESD..... Electo-Static Discharge
F2F ..... FPGA to FPGA
FAT..... Factory Acceptance Test
FE ..... Front End

FFT ..... Fast Fourier Transform
FN..... Front Node
FPGA ..... Field Programmable Gate Array
FW..... Firmware
GbE ..... Gigabit Ethernet
GTH ..... Gigabit Transceiver?
GUI..... Graphic User Interface
HDL ..... Hardware Description Language
HVAC..... High Voltage Alternate Current
HW ..... Hardware
ICD ..... Interface Control Document
IICD ..... Internal Interface Control Document
ILS ..... Integrated Logistic Support
INAF ..... Istituto Nazionale di Astrofisica
INAU..... Infrastructure Australia
INFRA ..... Infrastructure
INFRAAUS ..... Infrastructure Australia
I/O..... Input/Output
IP ..... Intellectual Property
IP ..... Internet Protocol
IP2, IP3 ..... Intercept point to 2nd and 3rd harmonic
ISO ..... International Organisation for Standardisation
IT ..... Information technology
ITF ..... Integration and Test Facility
LFAA..... Low Frequency Aperture Array
LFAA-DN..... Low Frequency Aperture Array – Data Network
LNA ..... Low Noise Amplifier
LMC..... Local monitoring and Control
LRU..... Line Replaceable Unit
LTP ..... Liquid Cold Plate
LVDS..... Low Voltage Differential Signal
M&C..... Monitor and Control
MAC ..... Media Access Control
MCCS ..... Monitor, Control and Calibration servers
MCU ..... Micro Controller Unit
MTBF..... Mean Time Before Failure
MTTR..... Mean Time to Repair
MTU ..... Maximum Transmission Unit
NTP ..... Network Time Protocol
OA ..... Operationally Capable
OHS ..... Occupational Health and Safety
ORX ..... Optical Receiver
OS ..... Operating System
PBS ..... Product Breakdown Structure
PCB..... Printed Circuit Board
PDR ..... Preliminary Design Review
PCA ..... Printed Circuit Assembly
PDS..... Power Distribution Subsystem
PFB ..... Polyphase Filter Bank
PHY ..... Physical (interface layer)
PLL..... Phase Locked Loop
PPE..... Personal Protective Equipment
PPS ..... Peak per second
PRR..... Product Readiness Review
PSN..... Packet Sequence Number

PSS	Pulsar Search
PST	Pulsar Timing
PWM	Pulse Width Modulation
QSFP	Quad Small Form Pluggable
RAL	Rutherford Appleton Laboratory
RAM	Reliability Availability and Maintenance
RD-n	nth document in the list of Reference Documents
RF	Radio Frequency
RFI	Radio Frequency Interference
RFoF	Radio Frequency signal over Fibre
RMON	Remote Network Monitoring
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances
RPF	Remote Processing Facility
SaDT	Signal and Data Transport
SAFe	Scaled Agile Framework
SDP	Science Data Processing
SFDR	Spurious Free Dynamic Range
SFP	Small Form Pluggable
SKA	Square Kilometre Array
SKA1	Square Kilometre Array Phase 1
SKA1-Low	SKA low frequency part of the full telescope
SKA1-Mid	SKA low frequency part of the full telescope
SKAO	SKA Office
SLD	Single Line Diagram
SMB	Subrack Management Board
S/N	Signal to noise
SNR	Signal to Noise Ratio
SOW	Statement of Work
SPEAD	Streaming Protocol for Exchanging Astronomical Data
SPI	Serial … Interface
SPS	Signal Processing Subsystem
SW	Software
TCP-IP	Transmission Control Protocol – Internet Protocol
TB	Transient Buffer
TBC	To Be Confirmed
TBD	To Be Decided
TCP	Transmission Control Protocol
TM	Telescope Management
TPM	Tile Processor Module
UCP	Uniboard Control Protocol
UDP	User Datagram Protocol
UTC	Universal Time Coordinated
VGA	Variable Gain Attenuator
VHDL	VLSI Hardware Description Language
WBS	Work Breakdown Structure
WDM	Wavelength Division Multiplexing
WEEE	Waste Electric and Electronic Equipment
XML	Extensible Markup Language

1 Introduction

1.1 Purpose of the document

The purpose of this document is to describe the Architecture for the Signal Processing System for the Low Frequency Aperture Array (LFAA) of the SKA Phase 1 with one detailed Reference Design implementation used to determine the envelope of its cost, power, equipment space, reliability, availability and maintainability.

1.2 Scope of the document

This document describes how the LFAA Signal Processing Sub-System reference design can meet the requirements within the SKA LFAA Signal Processing Requirement Specification [AD32] and meet or surpass the fidelity demonstrated in the SKA Signal Processing Sub-element Signal Model [RD57]

The level of detail in this document is sufficient to:

1. Define interfaces with other SKA Elements and LFAA Sub-elements.
2. Establish a reasonable reference baseline design at reasonably low perceived risk.
3. Estimate time, effort and cost to deliver the functionality specified in the LFAA Signal Processing Sub-Element Requirements Specification [AD32].

In other words, the LFAA Sub-Element reference design is defined in enough detail as to reduce risk of effort/time/cost overruns in the Construction Phase.

The current release (100% version) will support the Critical Design Review for the LFAA Element. The level of detail is enough to have high confidence in the reference design being compliant and able to be constructed with low risk. This Detailed Design Document (DDD), with references to supporting information and data, will provide a design artefact to support the Construction Phase activities.

Other potential implementations of the Signal Processing Subsystem which are included within the reference document folder [RD86]. This includes the Chinese Tile Processing Module, cTPM. This is not part of the reference design being reviewed at CDR but may be considered, along with other implementations, during the tender process.

1.3 Intended Audience

This document is expected to be used by the LFAA Element Consortium Engineering and Management Team and the SKAO System Engineering Team and SKAO LFAA Project Manager. This document is expected to be read by the external CDR review panel.

1.4 Telescope Overview

Figure 1 shows the major SKA1 Observatory entities: SKA1-Low in Australia, SKA1-Mid in South Africa and the SKA Global Headquarters in the UK. The thick flow-lines show the unidirectional transport of large amounts of digitised data from the antennas to the Central Processing Facilities (CPF) on the sites, and from the CPFs to the Science Data Processor (SDP) and Archive facilities. The thin blue dash-dot lines show the bidirectional transport of system monitor and control data.
The SKA1-Low telescope array includes 512 stations, each consisting of 256 dual-polarisation log-periodic antennas. The stations are distributed over 65 km, with the greatest density of stations in the

central core. The Central Processing facility is located on site and the SDP and archive are in Perth. Additionally, each station can be divided into several smaller sub-stations at reduced bandwidth.
A more detailed schematic of the SKA1-Low telescope, extracted from the SKA1 System Baseline V3 Description (in preparation), is shown in Figure 1-2. This figure shows the major SKA1-Low signal flow components, as well as the areas of consortia responsibility (red boxes) and the key technologies needed to implement the components. The green dashed line shows the bi-directional flow of monitor, control and operational data, and the orange dot-dashed line shows the distribution of synchronisation and timing signals.

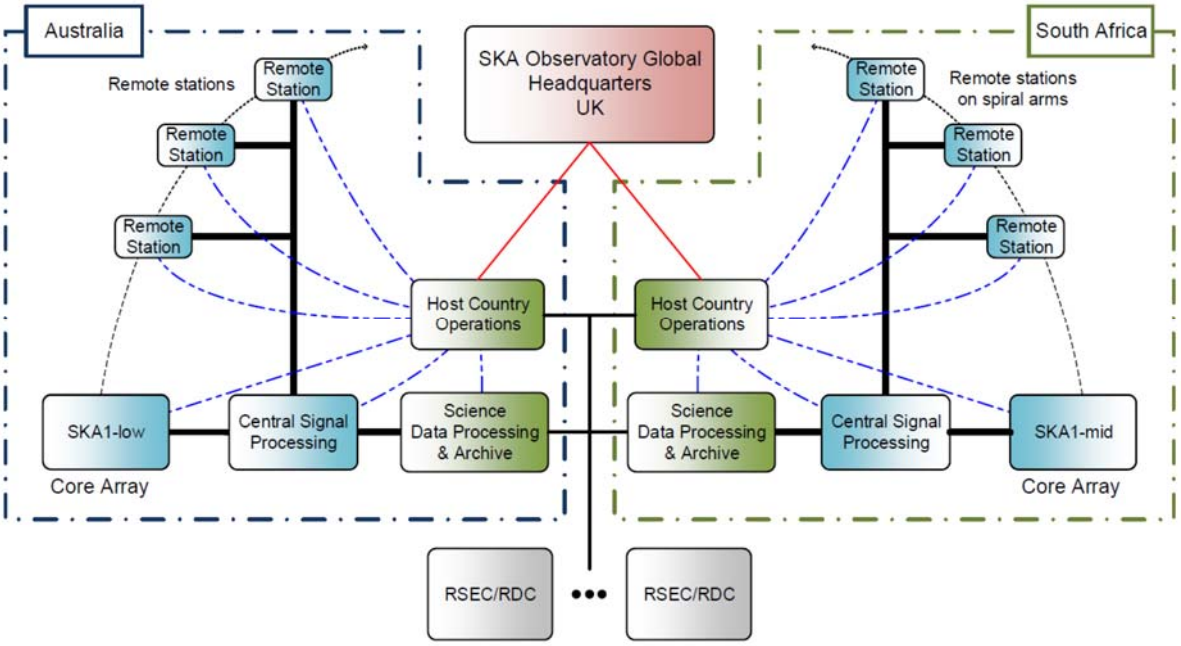


Figure 1-1 SKA1 Telescope Overview

A schematic of the SKA1_Low Telescope, extracted from the Baseline Design [AD5], is shown below including the LFAA Element, product [101-000000].

SKA1-Low operates concurrently in imaging mode and non-imaging mode with concurrent operation of between 1 and 16 sub-arrays. Each sub-array is programmable as a separate conceptual telescope in terms of antenna pointing, band selection and the setting of configurable imaging and non-imaging parameters. The only things that are shared between sub-arrays are observation time, communications links and processing resources.

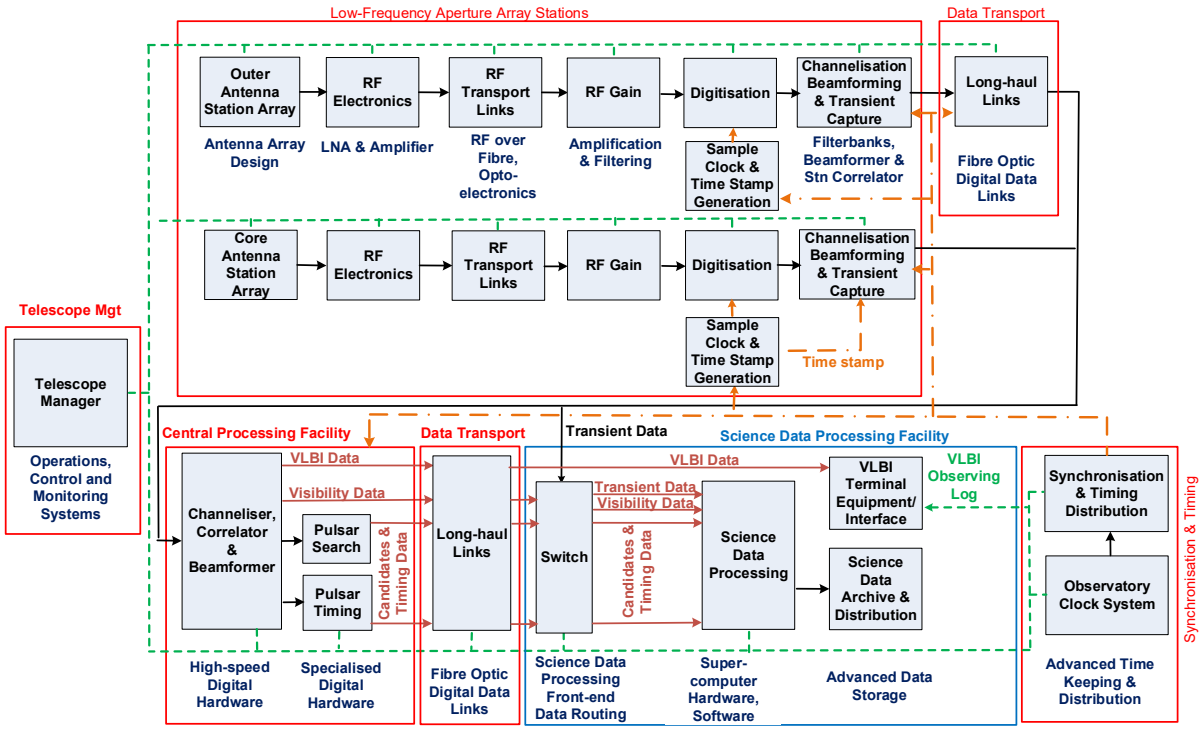


Figure 1-2 SKA1_Low Functional Diagram

1.5 Signal Processing System Overview

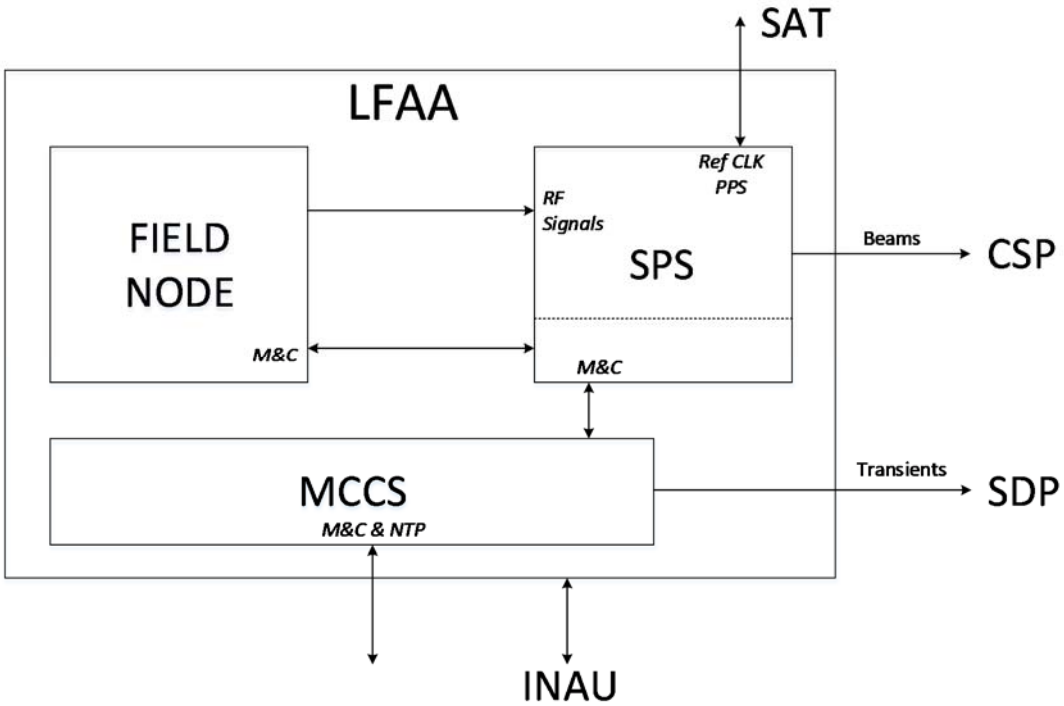


Figure 1-3 LFAA Sub-Elements

1.6 Document Overview

This document follows a template that was agreed to between the SKAO and the LFAA Consortium. It covers the key contents called out in the LFAA SOW [AD18].

Detailed information is provided in the appendices or is contained in reference documents.

1.7 Signal Processing System Scope

The key functions allocated to the Signal Processing System (SPS) are data acquisition and beamforming. These are described in Section 1.5. The key performance requirements allocated to SPS are described in Section 9.

The primary inputs to SPS are the dual polarisation RF signals from Field Node Antennas.

The scope of SPS does not include:

1. Calculation of beamforming calibration coefficients. These are supplied to SPS by MCCS [AD34]. SPS is responsible for applying these models to effect real-time coherent beam formation within accuracy and precision requirements.
2. Calculation of earth rotation delay polynomials for each antenna. These are supplied to SPS by MCCS [AD34]. SPS is responsible for applying these models to effect real-time delay and phase tracking within accuracy and precision requirements.
3. Making any decisions as to observation start time, stop time, or configuration. SPS responds to requests for such configurations but is itself simply a tool in the signal processing chain.
4. Making any decisions as to whether SPS equipment is powered on or off, except that SPS includes internal “deadman” thermal and overload protection that cannot be overridden.

1.8 Document Tree

The overall document tree for the LFAA Element is shown in Figure 1-4. Level 1 (L1) is the SKA System (telescope) level, L2 is the LFAA Element level and L3 is the LFAA sub-element level (where SPS resides).

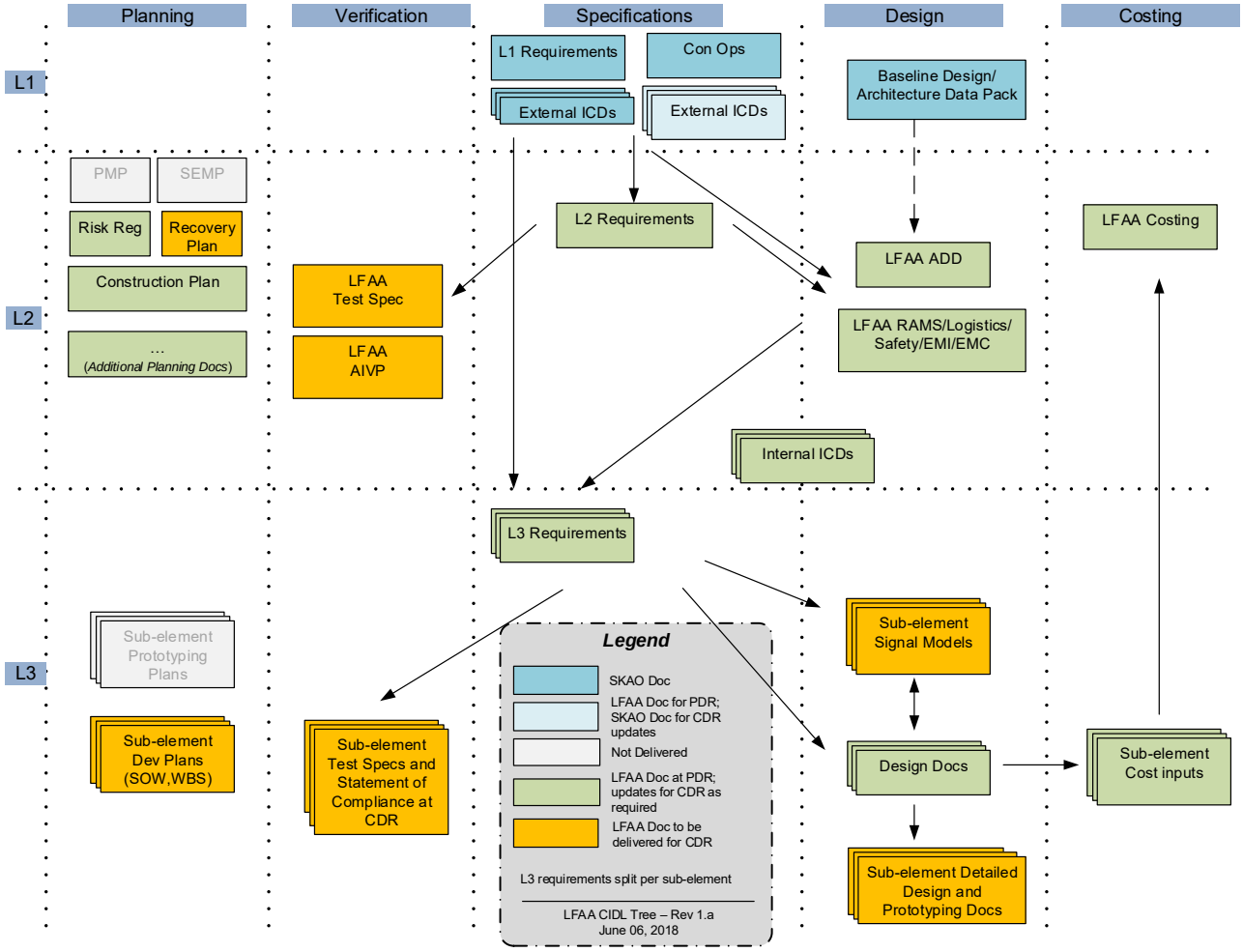


Figure 1-4 SKA1 LFAA Element Documentation Tree

2 References

2.1 Applicable documents

The following documents are applicable to the extent stated herein. In the event of conflict between the contents of the applicable documents and this document, **the applicable documents** shall take precedence.

[AD1] SKA Request for proposal Proposals SKA-TEL.-SKO-0000020 Issue 01
[AD2] Statement of work for the study, prototyping and design on a SKA element SKA-TEL.-SKO-0000021 Issue 01
[AD3] Statement of Work for the Study, Prototyping and Preliminary Design of a SKA Advanced Instrumentation Programme Technology SKA-TEL.-SKO-0000022 Rev 01
[AD4] SKA Pre-construction Top Level WBS SKA-TEL.-SKO-0000023 Iss 01
[AD5] SKA-1 System Baseline design SKA-TEL.-SKO-0000002 Iss 01
[AD6] The Square Kilometre Array Design Reference Mission: SKA Phase 1 SKA-TEL.-SKO-0000002 Rev 03
[AD7] SKA System Engineering Management Plan SKA-TEL.-SKO-0000024 Iss 01
[AD8] The Square Kilometre Array Intellectual Property Policy SKA-GOV-.POL-SKOPOL-001 Issue X
[AD9] LFAA Management and Organisation Agreement for the Aperture Array Design Consortium (AADC) AADC-TEL-LFAA-MGT.MGT-AADC-CNT-002 Iss 1A
[AD10] Document Requirements Description SKA-TEL.-SKO-0000029 Iss 01
[AD11] SKA Document Management Plan SKA-TEL.-SKO-0000026 Iss 02
[AD12] SKA Product Assurance and Safety Plan SKA-TEL.-SKO-0000027 Iss 01
[AD13] Change Management Procedure SKA-TEL.-SKO-0000028 Iss 01
[AD14] SKA Interface Management Plan SKA-TEL.-SKO-0000025 Iss 01
[AD15] SKA Phase 1 System (Level 1) requirements specification SKA-TEL.-SKO-0000008 Iss 08
[AD16] SKA Risk Management Plan SKA-MGT-RMT-MP-00001 Iss 01
[AD17] SKAO Project Management Plan SKA-TEL-SKO-0000159 Iss 01
[AD18] SKA1 LFAA Element Statement of Work
[AD19] SKA1 LFAA Architecture Design Document SKA1-TEL-LFAA-02000028 Rev 01
[AD20] SKA1 LFAA Signal Processing System Requirement Specification
[AD21] SKA1 LFAA to CSP Interface Control Document 100-000000-004 Rev 3
[AD22] SKA1 Field Node to SPS Sub-System Interface Control Document SKA1-TEL-LFAA-0200030 Rev 01
[AD23] SKA1 MCCS to SPS Sub-System Interface Control Document SKA1-TEL-LFAA-0200030 Rev 01
[AD24] SKA1 RAM Allocation SKA-TEL-SKO-0000102
[AD25] SKA LFAA EMI/ EMC Control Plan SKA1-TEL-LFAA-0200028 Rev 01
[AD26] SKA Logistics Analysis and Configuration Item Plan (To be provided by SKAO)
[AD27] SKA RFI Use Cases (to be provided by SKAO)
[AD28] Roll-out Plan for SKA1 Low SKA-TEL-AIV-4410001 Iss 05
[AD29] SKA Integrated Logistic Support Plan (ILSP) SKA-TEL-SKO-0000104 Iss 01
[AD30] SKA Support Concept SKA-TEL-SKO-0000103 Iss 01
[AD31] SKA RAM Allocation SKA-TEL-SKO-0000102 Iss 02
[AD32] SKA1 LFAA SPS Sub-Element Requirements Specification SKA-TEL-LFAA-0400014
[AD33] SKA1 LFAA Requirements Specification SKA-TEL-LFAA-0200026
[AD34] LFAA Internal ICD document SKA-TEL-LFAA-0200030 Rev 01
[AD35] LFAA to INFRA ICD 100-000000-003 Rev 03

[AD36] SKA1 Low SaDT to LFAA Interface Control Document 100-000000-026 Rev 04
[AD37] AAVS0.5: RFI Measurements and Updates A. Surtinio &F. Schlagenhaufer 13th March 2013
[AD38] SKA1 Low Configuration Constraints & Performance Analysis SKA-TEL-SKO-0000557 Rev 01
[AD39] SKA Power Budget SKA-TEL-SKO-0000035 Rev 05
[AD40] SKA Power Quality Standard SKA-TEL-SKO-0000293 Rev 03
[AD41] SKA EMI/EMC Standards and Procedures SKA-TEL-SKO-0000202
[AD42] LFAA System Engineering Management Plan AADC-TEL-LFAA-SE-MGT-AADC-PL-001
[AD43] LFAA Signal Processing System Test Specification SKA-TEL-LFAA-0500036

2.2 Reference documents

The following documents are referenced in this document. In the event of conflict between the contents of the referenced documents and this document, **this document** shall take precedence.

[RD1] SKA1 Control System Guidelines 000-000000-010 Iss 01
[RD2] Fundamental SKA Software and Hardware Description Language Standards SKA-TEL-SKO-0000661 Iss 02
[RD3] Introduction to Software Engineering Institute Processes for SKA Software CDR deliverables SKA-TEL-SKO-0000654 Iss 01
[RD4] The TANGO Control System Manual http://ftp.esrf.fr/pub/cs/tango/tango_92.pdf
[RD5] Documenting Software Architectures: Views and Beyond, Paul Clements et al., Pearson Education
[RD6] SKA1 Control System Guidelines - TANGO Naming Convention 000-000000-012
[RD7] RFI Characterisation and SKA1 Signal Chain Design Considerations SKA-TEL-SKO-0000492
[RD8] Management of alarms systems for the process industries, International Electrotechnical Commission IEC 62682
[RD9] Restriction of Hazardous Substances Directive (RoHS 2) http://www.conformance.co.uk/adirectives/doku.php?id=rohs Directive 2011/65/EU
[RD10] Waste Electrical and Electronic Equipment Directive (WEEE) http://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32012L0019 Directive 2012/19/EU
[RD11] IEC EN BS AS/NZS 60950-1 Information Technology Equipment - Safety Part 1 General Requirements
[RD12] Sanitas E.G.: “SKA LFAA SPS Cabinet Specification Document”
[RD13] Digital Signal Processing Requirements Compliance Matrix (included in Section **Error! Reference source not found.** in this document)
[RD14] Chiello, G. Comoretto: “TPM Firmware Architecture”
[RD15] G. Comoretto. C. Belli: “LFAA Tile Beamformer Signal processing”
[RD16] MIL-HDBK-217 F Reliability Prediction of Electronic Equipment 02 December 1991 http://www.sre.org/pubs/Mil-Hdbk-217F.pdf
[RD17] Telcordia SR-332 Reliability Prediction Procedure for Electronic Equipment May 2001
[RD18] IEC 60721-3-1 Classification of environmental conditions - Part 3: Classification of groups of environmental parameters and their severities - Section 1: Storage 1997
[RD19] IEC 60721-3-2 Classification of environmental conditions - Part 3: Classification of groups of environmental parameters and their severities - Section 2: Transportation 1997

[RD20] IEC 60721-3-3 Classification of environmental conditions - Part 3-3: Classification of groups of environmental parameters and their severities - Stationary use at weather-protected locations 2002
[RD21] ETSI EN 300 019-1-1 Environmental Engineering (EE); Environmental conditions and environmental tests for telecommunications equipment; Part 1-1: Classification of environmental conditions; Storage 2014 http://www.etsi.org/deliver/etsi_en/300001_300099/3000190101/02.02.01_60/en_3000190101v020201p.pdf
[RD22] ETSI EN 300 019-1-2 Equipment Engineering Environmental conditions and environmental tests for telecommunications equipment Part 1-2: Classification of environmental conditions Transportation http://www.etsi.org/deliver/etsi_en/300001_300099/3000190102/02.01.07_20/en_3000190102v020107a.pdf
[RD23] ETSI EN 300 019-1-3 Environmental Engineering (EE); Environmental conditions and environmental tests for telecommunications equipment; Part 1-3: Classification of environmental conditions; Stationary use at weather-protected locations http://www.etsi.org/deliver/etsi_en/300001_300099/3000190103/02.03.02_60/en_3000190103v020302p.pdf
[RD24] IEC EN 61000-3-2 Electromagnetic compatibility (EMC) - Part 3-2 - Limits - Limits for harmonic current emissions (equipment input current ≤ 16 A per phase) 2006+ A2 2009
[RD25] IEC EN 61000-3-3 Electromagnetic compatibility (EMC) - Part 3-3: Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current ≤ 16 A per phase and not subject to conditional connection Electromagnetic compatibility (EMC) - Part 3-3: Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current ≤ 16 A per phase and not subject to conditional connection 2017
[RD26] IEC EN 61000-4-2 Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test 2013
[RD27] IEC EN 61000-4-3 Electromagnetic compatibility (EMC)- Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test 2010
[RD28] EC EN 61000-4-4 Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test 2012
[RD29] IEC EN 61000-4-5 Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test 2014
[RD30] IEC EN 61000-4-6 Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields 2013
[RD31] IEC EN 61000-4-8 Electromagnetic compatibility (EMC) - Part 4-8: Testing and measurement techniques - Power frequency magnetic field immunity test 2017
[RD32] IEC EN 61000-4-11 Electromagnetic compatibility (EMC) - Part 4-11: Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests 2004
[RD33] IEC 61000-6-1 Electromagnetic compatibility (EMC) - Part 6-1: Generic standards - Immunity standard for residential, commercial and light-industrial environments
[RD34] IEC 61000-6-2 Electromagnetic compatibility (EMC) - Part 6-2: Generic standards - Immunity standard for industrial environments 2016
[RD35] IEC 61000-6-3 Electromagnetic compatibility (EMC) - Part 6-3: Generic standards - Emission standard for residential, commercial and light-industrial environments 2011

[RD36] IEC 61000-6-4 Electromagnetic compatibility (EMC) - Part 6-4: Generic standards - Emission standard for industrial environments 2011
[RD37] EN 55022 Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement 2010
[RD38] CISPR 22 Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement R2014
[RD39] CISPR 24 Information technology equipment - Immunity characteristics - Limits and methods of measurement 2010
[RD40] CISPR 32 Electromagnetic compatibility of multimedia equipment - Emission requirements 2015
[RD41] CISPR 35 Electromagnetic compatibility of multimedia equipment - Immunity requirements
[RD42] EUROPEAN POWER SUPPLY MANUFACTURERS ASSOCIATION RELIABILITY Guidelines to Understanding Reliability Prediction http://www.epsma.org/MTBF%20Report_24%20June%202005.pdf
[RD43] SKA1 Phase 1 System Requirement Specification SKA-TEL-SKO-0000008 Rev 11
[RD44] AS/NZS 1020:1995 Australian/New Zealand Standard: The control of undesirable static electricity 1995
[RD45] AS/NZS 1768:2007 Australian/New Zealand Standard: Lightning protection 2007
[RD46] AS/NZS 4836:2011 Australian/New Zealand Standard: Safe working on or near low-voltage electrical installations and equipment 2011
[RD47] AS/NZS 1319:1994 Australian/New Zealand Standard: Safety signs for the occupational environment 1994
[RD48] AS/NZS 5377:2013 Australian/New Zealand Standard: Collection, storage, transport and treatment of end-of-life electrical and electronic equipment 2013
[RD49] EN 55024 Information technology equipment. Immunity characteristics. Limits and methods of measurement 2010 + A1:2015
[RD50] AS/NZS 3000-2007 Wiring rules
[RD51] AIV Roll-out Plan SKA-44100001
[RD52] LFAA Risk Register SKA-TEL-LFAA-0000009
[RD53] LFAA Signal Processing System Prototyping Test Report SKA-TEL-LFAA-0500047
[RD54] LFAA Costing Spreadsheet SKA-TEL-LFAA-0000004
[RD55] LFAA Logistics Report SKA-TEL-LFAA-02000044
[RD56] LFAA Hazard Analysis SKA-TEL-LFAA-00000024
[RD57] Signal Modelling SKA-TEL-LFAA-0500048 Rev 01
[RD58] SPS Technical Performance Measures (TPM) spreadsheet
[RD59] SKA RFI Use Cases (to be written by SKAO)
[RD60] MCCS Software Architecture Document SKA-TEL-LFAA-0600052
[RD61] LFAA tile processing module programming manual, Arcetri internal report 2/2018
[RD62] MCCS Detailed Design Description SKA-TEL-LFAA-0600051
[RD63] SKASystemBudget LowSystemTimingBudget_u1 SKA-TEL-SKO-0000637-03
[RD64] ADU User Manual (Sanitas)
[RD65] Design of performance improvements and industrial process of SKA-LFAA receiver (LEONARDO)
[RD66] SKA Management Board Description (Sanitas EG)
[RD67] AAVS0.5 : RFI Measurements & Updates (ICRAR-2013)
[RD68] Detailed Thermal Study Cooling Solution for SKA (AAVID)
[RD69] Australian Health and Safety Act
[RD70] LFAA Hazard analysis This report section 11.1
[RD71] SPS power supply specification for TPM Sub-rack unit

[RD72] SKA LFAA conceptual sub-rack design (Sanitas)
[RD73] Clock distribution analysis (Sanitas)
[RD74] Technical Report SKA LFAA Reliability Study Receiver (Università di Firenze - LEONARDO)
[RD75] Availability Study Receiver (Università di Firenze - LEONARDO)
[RD76] Thermal stress FEM (Università di Firenze)
[RD77] ADU Board Test Plan (Sanitas)
[RD78] ADU Board Test Procedure Document (Sanitas)
[RD79] LFAA Tile Beamformer structure, Arcetri internal report 2/2015
[RD80] LFAA Station Beamformer structure, Arcetri internal report 5/2016
[RD81] LFAA tile beamformer functional model, Arcetri internal report 6/2017
[RD82] Quantization effects and nonlinearities in multi-bit correlation, Arcetri internal report 4/2018
[RD83] Management board reliability analysis, Università di Firenze – Dipartimento di Ingegneria dell'Informazione RR03-18
[RD84] Cabinet Monitor and Control Points - Sanitas EG report (2018/09/10)
[RD85] SKA LFAA conceptual sub-rack design Sanitas EG Iss 1.2 14/02/2018
[RD86] Signal Processing Sub-system Reference Folder SKA-TEL-LFAA-0500055

3 Operational Concepts

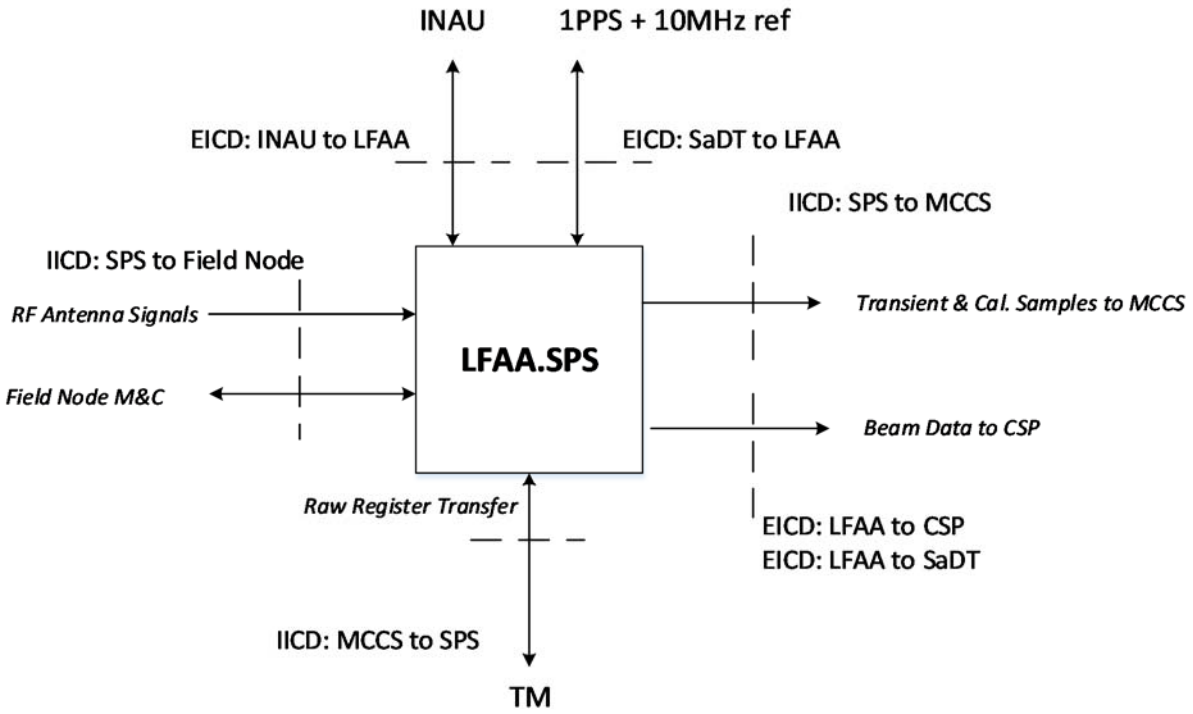


Figure 3-1 SPS Sub-Element top-level context diagram showing all external interfaces

3.1 Operational Environment

The Central Processing Facility (CPF) screened room and Remote Processing Facilities (RPFs) will house the SPS equipment as well as other surrounding/support equipment such as that used for SaDT timing and networks, the CSP correlator and LFAA MCCS.
The CPF and RPFs are RFI-shielded facilities supporting liquid cooling. These facilities have some level of ESD protection and has HVAC filters to prevent dust accumulation on equipment. Notwithstanding the RFI-shielded facility, LFAA LRUs, including those comprising SPS, are required individually to meet CISPR-22/32 Class A [RD38]/[RD40] radiated and conducted emissions levels. Additionally, SPS LRUs must meet CISPR 24/35 [RD39]/[RD41] Class A radiated and conducted susceptibility levels or equivalent. This is described in more detail in Section 12.3.3

3.1.1 Operations

During normal operations SPS is controlled via the interface with MCCS [AD34]. SPS implements a high-level interface which allows the MCCS to control and monitor SPS as a single instrument. A single point of access is provided for housekeeping commands such as power-up, power-down, and state and mode transitions. Monitoring and error reporting are subscription-based; all parameters that may be of interest to MCCS, TM, and operations in general, including the rolled-up overall operational state and health, are available for subscription. In addition, the SPS monitor and control interface provides introspection, i.e. allows an authorised client to 'discover' and access parameters and commands implemented by the lower level components when required to support diagnostics and maintenance. Signal processing functions are controlled via sub-arrays and scans. SPS supports sub-arraying, i.e. provides high-level commands [AD34] that MCCS can use to sub-divide the Low Telescope into up to 16 sub-arrays and operate each sub-array independently. SPS exposes sub-arrays as top-level entities

and makes provision for MCCS to assign antennae to sub-arrays and select signal processing functions to be performed per sub-array.
A scan is defined as a time interval during which a sub-array's configuration does not change. During normal operations, MCCS accesses a sub-array directly to assign antennae, select signal processing functions, as well as start and stop the scan (i.e. start and stop signal processing).
Normal operational scenarios with the SPS system are described in Section 7.

3.1.2 Maintenance

The SPS Sub-element is an IT system with some specialised features. It therefore requires typical data centre/IT system maintenance but with specialisation for the analogue RF based pre-ADU and FPGA based ADU LRUs. Thus, maintenance personnel will be a mixture of typical IT-support personnel and specialised/specially-trained support personnel; normally only typical IT-support personnel are expected to be required at the site itself.
Maintenance is described further in Section 16.1

3.1.3 Operator Role

Apart from maintenance activities, LFAA (and thus SPS) is remotely controlled via TM and ultimately by an operator within the TM environment.
The "operator"/maintainer role and how it relates to SPS is described in more detail in Section 16.5.1.

3.2 Support Environment

Support for SPS will be provided both on-site (i.e. Boolardy) and off-site (i.e. at the SKA1_Low Telescope support facility at Geraldton and/or in/near Perth), as well as remotely.
On and off-site support is described in more detail in Section 16.1.1.

3.2.1 On-site Maintainer role

The SPS on-site maintainer needs a technical hardware support background as described in Section 16.1.1 to execute the required maintenance tasks.
This maintainer's primary objective is to detect and isolate faulty LRUs (corrective maintenance) and to remove and replace these to restore the SPS functionality. The maintainer's secondary objective is to determine what maintenance needs to be scheduled (predicted and preventative maintenance) and to coordinate and perform the required tasks when scheduled.

3.2.2 Off-site Maintainer role

The off-site maintainer needs software/hardware technical support background to perform second line bespoke LRU repairs, configuration, and verification as described in Section 16.1.1.
The off-site maintainer is located at the SKA1_Low Telescope support facility. The off-site maintainer removes and replaces selected SRUs to repair bespoke LRUs, configures the repaired bespoke and COTS LRUs, and tests all repaired equipment in a representative environment to verify that they are fully operational. Once this is confirmed, LRUs are returned to the on-site or close-to-on-site spares store.

3.2.3 Remote support

SPS maintenance and support personnel will remotely connect to the CPF over the SKAO communication network to read equipment status, review equipment log files and access SPS long term monitoring data that is stored in the TM Engineering Data Archive (EDA), to help isolate faults.
Off-site support is generally more specialised, and hence is preferred to detect and isolate faults. Off-site support will be provided where possible to assist the Telescope on-site operations personnel to diagnose faulty LRU equipment and problems with telescope functionality (firmware and software).
The general rule is, if something can be done remotely, it should be done remotely, but with on-site capability and assistance if such capability is useful (e.g. GUIs on consoles to track down problems).
See Section 16.1.1.2 for more information on remote support.

3.3 States and Modes

The SPS implementation of states and modes is compliant with the SKA Control System Guidelines document [RD1]. Per these guidelines, SPS implements and reports the standard set of SKA state and mode indicators for the SPS and for individual sub-arrays. Table 3-1 and
Table 3-2 provide an overview of the most significant state and mode indicators implemented for SPS and SPS sub-arrays.
In addition, SPS implements and, upon request, reports the standard set of states and modes for major components at several levels of the monitor and control hierarchy, as applicable.

MCCS monitors SPS state and mode transitions and based on the status reported by SPS derives overall LFAA state and mode indicators.

Attribute	Range	Description and comments
adminMode (read-write)		Set by an outside authority (operations via TM/MCCS), the value reflects how operations wants to use SPS.
	ONLINE	SPS can be used for observing (scientific or other).
	MAINTENANCE	SPS should not be used for scientific observing. Note: SPS is not aware of the higher observation goals (science vs testing) and does not enforce this restriction – it is up to operations and TM to enforce this rule. However, SPS can be set in a system-level Test Mode only when adminMode=MAINTENANCE. MAINTENANCE is the factory default; when commissioning is completed operations should set adminMode=ONLINE.
	OFFLINE	SPS should not be used at all.
	NOT_FITTED	Set by operations to suppress alarm generation.
opState (read-only)		SPS intelligently rolls-up the operational state and other indicators for all hardware and software components and reports the overall operational state.
	OFF	Power is disconnected (cannot be reported by SPS itself).
	INIT	The software running on the SPS Control Server and the equipment used for the monitor and control network are being initialised.
	STANDBY	Low-power state. SPS uses < 5% of nominal power; basic monitor and control functionality is available.
	ON	Normal operational state. SPS enters this state when at least a minimum of SPS signal processing capability is available: at least one antenna and one sub-array can be used for observing (either for scientific observations or for testing and maintenance). Operational availability can be detected via other indicators, such as healthState, availability of capabilities and components, etc.
	ALARM	The Quality Factor for at least one attribute is outside the pre-defined ALARM limits. Part of SPS functionality may be unavailable.
	DISABLE	SPS is administratively disabled, either by setting adminMode OFFLINE or NOT_FITTED, or via a command to transition to state=DISABLE. Basic monitor and control functionality is available, but signal processing functionality is not available.
	FAULT	An unrecoverable fault has been detected. SPS is not available for use at all. Maintainer/operator intervention is required in order to return to ON, STANDBY, or DISABLE.
	UNKNOWN	SPS is unresponsive, e.g. due to communication loss (cannot be reported by SPS itself).

Attribute	Range	Description and comments
healthState (read-only)	OK DEGRADED FAILED	SPS intelligently rolls-up attribute quality factors, availability, and other indicators and reports overall SPS healthState. Components where adminMode=NOT_FITTED or OFFLINE are excluded from the roll-up. Note: The healthState reported by SPS indicates health as detected by the SPS itself and is one of the inputs for calculation of the overall operational availability, which in some cases cannot be determined in real-time.

Table 3-1 SPS States and Modes

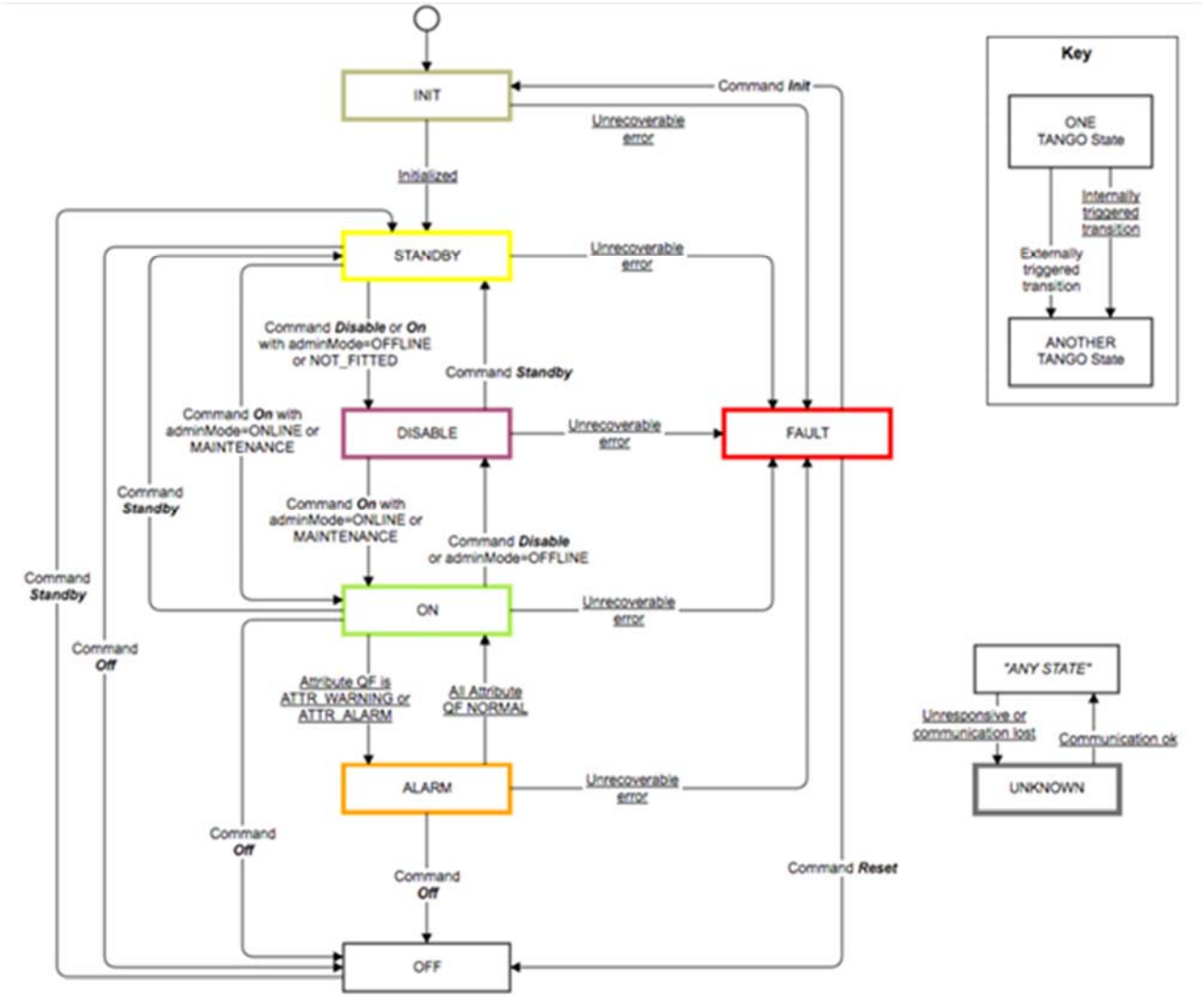


Figure 3-2 SPS Operational states

Attribute	Range	Description and comments
adminMode (read-write)		Set by an outside authority (operations via TM and MCCS.LMC).
	ONLINE	The sub-array can be used for scientific observing.
	MAINTENANCE	The sub-array is not to be used for scientific observing but can be used for testing and commissioning.
	OFFLINE	The sub-array is not to be used at all.
	NOT_FITTED	Set by operations to suppress alarm generation.
opState (read-only)		SPS intelligently rolls-up the operational state of all components used by the sub-array and reports the overall operational state for the sub-array.
	INIT	The sub-array is being initialised.
	OFF	The sub-array is 'empty'; no receptors have been assigned to the sub-array.
	ON	At least one receptor has been allocated to the sub-array; the sub-array is ready to accept a scan configuration.
	ALARM	The Quality Factor for at least one attribute is outside the pre-defined ALARM limits. Some or all functionality may not be available.
	DISABLE	The sub-array is administratively disabled (adminMode=OFFLINE or NOT_FITTED); basic monitor and control functionality is available, but signal processing functionality is not available.
	FAULT	An unrecoverable fault has been detected. The sub-array is not available for use; maintainer/operator intervention is required.
	UNKNOWN	The sub-array is unresponsive, e.g. due to loss of communication.
healthState (read-only)	OK DEGRADED FAILED	SPS intelligently rolls-up attribute quality factors, states, and other indicators for all components and capabilities used by the sub-array and reports the overall sub-array healthState.
obsState (read-only)		The sub-array Observing State indicates status related to scan configuration and execution.
	IDLE	The sub-array is not processing input data and is not generating output products. When a sub-array is IDLE, SCAN ID=0.
	CONFIGURING	Transient state entered when a command to re-configure the sub-array is received. The sub-array leaves this state when re-configuration is completed.
	READY	The sub-array enters READY when re-configuration has been completed.
	SCANNING	The sub-array is processing input data and generating output products.
	ABORTED	The sub-array transitions to this state when a command 'abort scan' is received. In this state re-configuration, delay tracking, and any other on-going processing functions are stopped.
	FAULT	An unrecoverable error that requires operator intervention has been detected.

Table 3-2 SPS States and Modes Detail

4 Assumptions and Risks

4.1 Assumptions

Below is a list of assumptions that were made during the design activities for SPS. These are in addition to assumptions made with regards to requirements, which are given in the LFAA Level 2 Requirements Specification [AD33] and in the SPS L3 Requirements Specification [AD20]. The list of assumptions below also does not cover items in the SPS Technical Performance Measures (TPM) spreadsheet [RD58].

ID	Category	Assumption	Resolution Plan
1	Design Constraint		
1.1		Power use should be minimised whilst a) meeting functional and performance requirements and b) staying within an agreed budget allocation Medium risk – of the SPS exceeding the allocated power budget. Renegotiate budget and if this is not feasible some redesign may be required with potential cost impact.	
1.2		Physical implementation should be amenable to a technology refresh to save cost and power with a minimal re-design effort. Low -risk	
2	Environmental Conditions		
2.1		Temperature inside the cabinet constant Low -risk: Analogue & ADC gain fluctuation vs temperature.	Optimised temperature controller for the cabinet
2.2		SPS equipment is EMC compliant Medium risk - All the electronics has been designed with “good engineering practice for EMC” but it needs to be tested. Redesign some parts if there is no compliance	Prototype and verify for EMC compliance
3	Analysis & Calculation Conditions		
3.1		The reject-band attenuation in any band-pass filtering is sufficient.	Release of SKA RFI Use Cases [RD59]

		Medium risk – higher attenuation in the reject band could require larger FPGAs. This would have cost implications particularly if redesign is required to match component footprint	
3.2		Planned temporal RFI mitigation method (Section 6.8) is sufficient for RFI flagging (REQ-198) Medium risk – more advanced RFI flagging algorithms could require larger FPGAs. This would have cost implications particularly if redesign is required to match component footprint	Release of SKA RFI Use Cases [RD59]
3.3		Linearity compliance High risk - necessary to evaluate where non-linearities are generated. Analogue chain: modify antenna performances (low frequency response), redesign filters stages increasing stopband attenuation, modify LNA passband and/or dynamic range, increase the linearity of last analogue amplifiers Digital part: ADC performances, increase the of bits for acquisition	Release of SKA RFI Use Cases [RD59] Finalise Antenna/LNA design
4	Maintenance Conditions		
4.1		TPM, sub-rack management, and cabinet management LRUs are repaired (and can be repaired) rather than discarded; the number of assemblies that can't be repaired over a 20-year lifetime is less than the number of spares (10%) Low risk – the number of failures that cannot be repaired is expected to be small. If that is not the case, OPEX costing may not be sufficient	Ops/ maintenance budget + plan finalised.
4.2		Any LRU repair facility is security-certified to minimise the possibility of the introduction of a malicious computer virus.	Ops/ maintenance budget + plan finalised

		Low risk – should be standard for a repair facility dealing with hardware, firmware and software	
4.3		LFAA.SPS LRUs will only be opened/ repaired at a facility with certified ESD handling capability. Low risk – standard practice for high value IT equipment	Ops/maintenance budget plan finalised.
5	Access Constraints		
5.1		Authentication for network access to LFAA.SPS equipment from any location other than inside the CPF and RPF facilities is provided by another Element (i.e. other than LFAA) Medium risk – details are still TBD on access and authentication. If this becomes a LFAA.SPS responsibility it will impact construction cost and schedule	Ops/ maintenance budget + plan finalised
5.2		Only qualified and trained personnel will have access to the LFAA.SPS system in the CPF and RPFs Low risk – standard practice for high performance IT facility	Ops/ maintenance budget + plan finalised
6	Interface TBDs	All the interfaces should be based on commonly used standard interfaces Low risk	

Table 4-1 SPS Assumptions, associated risk and retirement plan

4.2 Risks

The assumptions listed above (and in the requirements documents as noted) all carry some risk until they are resolved as described in the Retirement Plan column. In addition to these risks, technical and programmatic risks are described in the LFAA Risk Register [RD52] and mitigation activities are discussed in the SPS Prototype Test Report [RD53].

5 SPS Architecture Description including Physical Description

In this section the architecture of the Signal Processing Subsystem is introduced. Initially a functional description of the subsystem is presented.

5.1 SPS Overview

5.1.1 Functional

The SPS's key function is to combine the signals of a field node into one, or more, station beams, for 512 stations (L3-184), separated by up to 65 km (L3-185). The purpose of the beamforming function is to provide to the central beamformer a signal that is logically equivalent to that of a single radio receptor, with a collecting area that is the sum of those of the field node antennas, steered to the region(s) of interest in the sky.
The primary functions of the LFAA.SPS are:

- To receive the RF signals generated by the individual antennas. Signals are received on optical fibres, converted to an electric signal, filtered to select the required RF band (L3-173) and amplified.
- To digitise the RF signals (L3-174). Digitisation also associates the RF samples with precise timing information (L3-179), derived from the reference clock and the distributed Pulse per Second, PPS, signal.
- To participate in the frequency channelisation of the received signal, providing CSP with channels of appropriate bandwidth, oversampling (L3-208), channel spacing and frequency response (L3-181, L3-182, L3-202). Channels partially overlap, with a highly uniform spectral response over the not overlapping portion of each channel (L3-183). This allows a seamless reconstruction of the original signal spectrum.
- To calibrate these signals according to MCCS calibration information. Calibration includes components relative to the complex receiver gain, antenna gain, atmosphere, polarization impurities, ionospheric Faraday rotation, parallactic rotation, antenna tapering for beamforming (L3-189) and a bandpass equalisation to optimise the signal amplitude across the received band.
- To combine the signals of one or more substations, up to 256 antennas total, into one or more beams (L3-178). Geometric delay in the pointed direction is corrected in the frequency domain, using a linear phase correction (delay and delay rate) updated every few seconds. Up to 8 different pointing directions can be specified (L3-177), for a total aggregate bandwidth of 300 MHz covering arbitrary, overlapping or not overlapping, regions (L3-201).
- To generate calibration sample spigots for the MCCS. These include signals for all antennas and polarisations, for one spectral channel at a time. MCCS derives antenna calibration coefficients from cross correlating these samples, with enough time and spectral resolution to guarantee specified coherence in the station beamforming process.
- To generate a stream of beamformed samples for selected antennas and frequency channels, to be stored in the fast-transient events buffer. Samples are a 2-bit version of the samples sent to CSP, for up to 150 MHz of total bandwidth (L3-204). Transient sample capture can be started and stopped at commanded times.
- To identify and flag samples affected by RFI (L3-198) or saturated in the signal processing chain (L3-200), also using flagging information from TM (L3-199).
- To generate monitor information (L3-125), including total power data for individual antennas, integrated spectra for one antenna (in turn) (L3-180), partial beam, station beam, thermal status, power status (L3-190), and interface diagnostics (L3-186).

- To provide self-test capabilities for fault diagnostics. During observations (scanning mode) the system checks for FPGA configuration memory soft errors (L3-120), Ethernet interface status, memory errors and power level anomalies (L3-190, L3-121, L3-122, L3-123, L3-124). In offline mode it is possible to generate test signals and to check for the expected results (L3-116). It should be possible to isolate the faulty element to LRU level (L3-117, L3-118, L3-119), to guarantee a fast repair (L3-114).

5.1.2 Non-Functional

To implement the functionalities outlined above, SPS must also provide:

- Electric power distribution to all its elements, with power quality conforming to the LFAA-INAU ICD (L3-149, L3-150, L3-151, L3-152, L3-153, L3-154, L3-155, L3-156, L3-157, L3-158, L3-159, L3-163, L3-164, L3-167)
- Thermal power removal to the infrastructure cooling liquid circuit described in the LFAA-INAU ICD (L3-167, L3-197)
- Power supply management, allowing individual elements to be powered on and off, and/or placing them in low power mode (L3-31, L3-32). SPS basic monitor and control functions are always available in any power mode (L3-33)
- Mechanical housing (SPS cabinet) for the SPS equipment, both in the CPF building and RPF sites (L3-193, L3-194). A total of 148 cabinets will be present in the CPF, and 3 in each of the 36 RPFs (L3-195).
- Mechanical housing (splicing cabinet) for the mechanical interface between the FN optical fibres and the SPS optical fibres according to FN-SPS IICD (L3-191)
- RF optical fibre transport from the splicing cabinet to the SPS cabinet
- Network optical fibre transport of beamformed data to CSP (L3-145)
- For remote stations, data transport to/from the SaDT interface points, both at the remote side and at the core building (L3-146).
- Electronic and human readable identification of all LRUs (L3-138, L3-139, L3-140, L3-133), cables (L3-142), connector plates (L3-142) and packages (L3-141)
- Labelling of equipment for safety markings (L3-99), hazards (L3-101), heavy equipment (L3-100), disposable equipment (L3-104) and ESD warning labels (L3-98), with long lasting labels (L3-102)
- Protection against power failures (L3-172, L3-97)
- MCCS LMC network distribution to SPS elements, with network partition and routing management (L3-191)
- MCCS LMC network distribution to FN, using two of the spare optical fibres in the FN-SPS optical cable (L3-191)
- Guarantee instrument safety (L3-68, L3-47, L3-69, L3-48), fail safe warnings (L3-49), fail recovery (L3-50),
- Thermal and overcurrent dead-man safety protection (L3-95)
- Compliance with all local health and safety regulations (L3-73, L3-168, L3-169, L3-170, L3-171, L3-65), and operator safety (L3-89, L3-90, L3-91. L3-92, L3-93, L3-94, L3-96)
- Compliance with all environmental regulations (L3-63, L3-105), recycling regulations (L3-103),
- Adequate protection against RFI emission and susceptibility (L3-160, L3-161, L3-162, L3-164, L3-165, L3-106, L3-107, L3-108, L3-109, L3-110)
- Initial programming of all programmable devices, including in-system remote programming updates (L3-126, L3-127, L3-115)
- Easy access and substitution of all LRUs (L3-128, L3-129, L3-130, L3-131, L3-132)
- Hardware and communication access control (L3-144)

- Storage space in a weather protected environment for spare parts and maintenance equipment (L3-134), part package (L3-135)

The SPS provides cabling for signal and data transport for:

- RFoF signals, from the splicing cabinet to the SPS cabinets
- Beamformed data, from SPS cabinets located in the CPF to CSP cabinets (L3-145, LFAA-CSP ICD)
- Beamformed data, from SPS owned long haul switches in the CPF to CSP cabinets (L3-145, LFAA-CSP ICD)
- Any necessary cables between SPS cabinets located in the RPFs and the SPS owned long haul switches in the RPFs.

SPS will not provide cabling for signals between MCCS and SPS cabinets, or SPS owned long haul switches in the CPF. These cables are part of the MCCS PBS (L3-192, MCCS-SPS IICD).

5.2 SPS Architecture Overview

SPS basic structure is shown in Figure 5-1.

The main sub-system of the signal processing is the Tile Processing Module, TPM. This is a rack-mounted unit that processes the signals from 16-antennas (32-signal chains). The TPM receives the analogue signals from the FN RF antenna amplifiers, as analogue RF over Fibre optical signals, amplify and filter them (RF conditioning), convert them in digital form and digitally process them to form station beams. 16 Tile Processing Modules related to one station are connected using a high-speed data switch. Partial beams are sent along a chain of 16 TPMs, with each TPM combining the internally generated partial beam with the travelling one. The final station beam is then sent to the CSP.

The data switches are used also to interface the TPM to the MCCS, both for local monitor and control functionalities and for sending to MCCS calibration samples spigots, and samples to be stored in the transient buffer.

SPS is physically implemented in 256 cabinets. Each cabinet hosts 32 TPMs and 2 data switches, for two stations, plus the necessary power, cooling, clock distribution and management hardware.

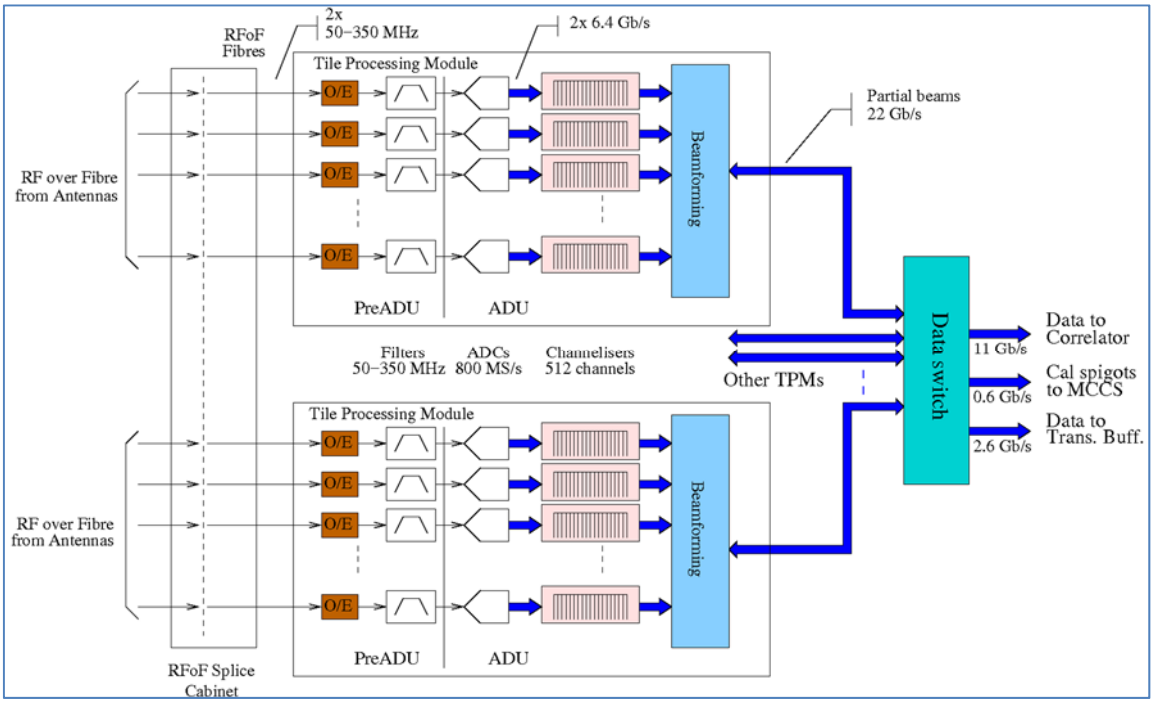


Figure 5-1 Block description of the TPM-ADU

Figure 5-2 outlines the data flow and top-level signal processing functionality implemented in the TPM-ADU with the requirements formalised in RD20. All the processing illustrated takes place within the signal processing devices on the TPM-ADU.

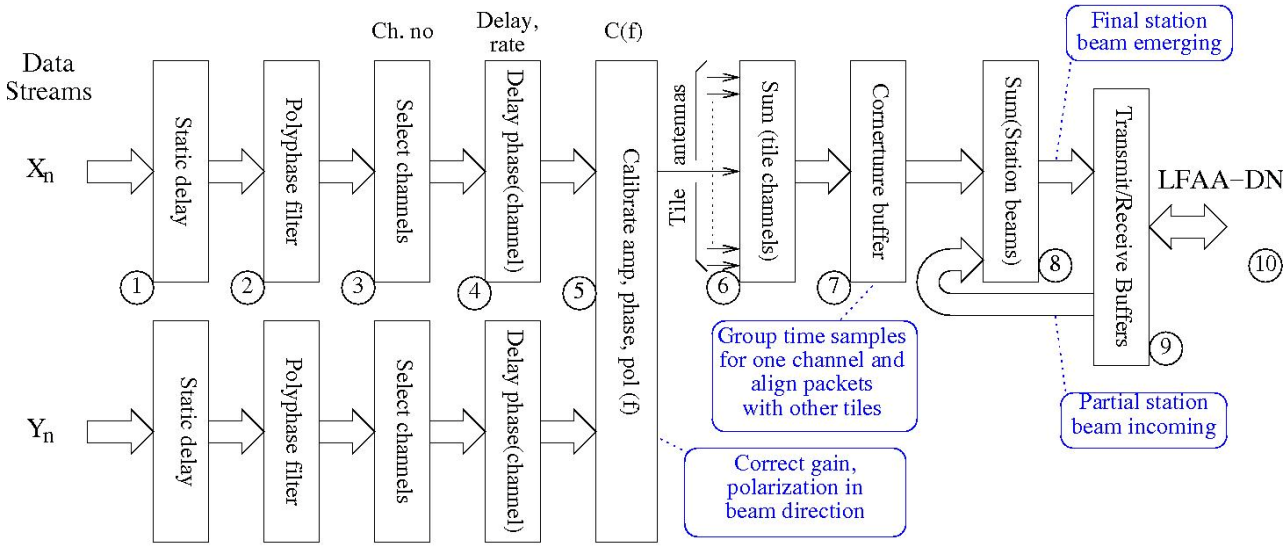


Figure 5-2 Outline processing flow for Tile and Station beamforming. See text for explanation of step numbers

The signal processing for the antennas on the digital tile processors is to:

1. Digitise the analogue signal using 7.8-bit (ENOB) high speed digitisers, which can accommodate the likely RFI levels. Sampling period is 1.25 ns (800 MHz sampling frequency);
2. Correct for static delay ① due to cable mismatch: frames from each antenna are delayed by ±128 samples. Samples are nominally aligned to ±1/2 sample for a radio source placed at the zenith;

3. Channelise ② the bandwidth into 512 overlapping channels, with centre frequency spaced by 781.25 kHz and sample period of 1.08 μs, for a phase shift-controlled delay approximation in the beamforming as suggested in AD19
4. Select the frequency channels ③ for each beam being formed (a specific frequency channel can be selected multiple times);
5. Apply appropriate beamformer phase ④, derived from specified delay and delay rate, to each select frequency channel sample;
6. Calibrate the signal as a function of frequency to compensate for bandpass errors, gain and phase; and correct the polarisation ⑤by each frequency channel and pointing direction with a matrix multiply between polarisation samples using complex correction matrix C(f); This also includes the amplitude for the appropriate beamformer weights to each select frequency channel sample; after this stage samples for both polarisations are treated in parallel;
7. Sum all 16 antenna signals into a tile beam or beams ⑥, and requantised to 12 bits.

The ADU Tile processor sums an incoming partial beam from previous tile processors, illustrated in Figure 5-2, with the tile beam formed locally as follows:

8. The tile beam samples formed above are delayed in a memory buffer ⑦ by the appropriate amount to align with an incoming partial beam. The buffer also performs a corner-turner operation grouping consecutive time samples for each channel.
9. A partial station beam, formed from the summing of other tile processors, is routed to this tile processor ⑨.
10. The tile beam(s) formed by this tile processor is summed ⑧ with the incoming partial station beam(s).
11. The partial or complete beam(s) formed is then sent, via the 40 GbE interface, to the data network ⑨ for routing either to the next ADU Tile Processor or to the LFAA correlator.
12. The beamformed station signal is then requantised to 8 bit and sent to the CSP ⑩.

5.2.1 Control and Monitoring Functions

The two primary functional requirements of the software infrastructure of LFAA, including the software components of SPS, are:

1. The creation and monitoring of observations
2. The provision of monitoring and control capabilities for all the hardware and software components

MCCS is responsible for hosting the software infrastructure, including most of the elements which directly monitor and control SPS hardware and firmware. An overview of the software architecture for MCCS, and hence LFAA, is described in [RD60], whilst the software architecture itself is described in greater detail in [RD2]. TANGO has been adopted as the primary SKA-wide control framework, such that each monitorable and/or controllable hardware device in SPS has an associated TANGO device through which all operations are performed, including TPMs, antennas, APIUs, switches, rack management boards and other cabinet equipment. These TANGO devices will run on the MCCS servers and communicate with their associated hardware components through appropriate protocols. Standard or proprietary protocols will be adopted for COTS hardware, while an interfacing Application Programming Interface (API) is defined for the TPM and described in [RD61].**Error! Reference source not found.**

5.2.1.1 *Monitoring*

In this context, monitoring refers to the act of reading device attributes (such as sensors, status flags and firmware status registers) without affecting the device operation.
These attributes can include:

a. Internal temperature (including the temperature of sub-elements in an LRU)
b. Voltage
c. Power consumed
d. Cooling mechanism status
e. Communication path status
f. Device configuration status
g. Device status

Attributes a to d can be monitored if the device has the required sensors. The communication path status is more complex, since to locate a fault in a link all intermediary devices must be checked, and thus requires a good mapping of how the hardware components are connected. This is described in [RD60] Section 7. Device configuration is generally retrieved from the device (if possible) and cached in the associated TANGO device. This is updated during re-configuration or when a control command which affects this configuration is issued. Device status is updated when a fault is detected, the device is unreachable, or an operation is performed which changes the device state, such as when configuring and starting and observation.

5.2.1.2 *Configuration and control*

Device configuration is performed at two instances:

- The device is switch on. Some device, like the TPM, are placed in low power mode, where a minimal configuration is required. Other device, like network switches, are fully configured on start-up. Default configuration for each device is retrieved from the LFAA Configuration Database, as described in [RD62] Section 6.2
- During observation configuration. All devices contributing to an observation must be put in the READY state. This is mostly applicable to the TPM, which must be programmed, initialised and configured, which includes setting up the channeliser with channel scaling factors and calibration coefficients, setting up the beamforming chain and applying pointing delays. Calibration coefficients, channel scaling factor and pointing delays are routinely updated during an observation. Observation management is described in detail in [RD60] Section 5

Configuration commands are a subset of the control commands required. Additional commands include power control, communication path management and maintenance-specific functionality.

5.2.1.3 *Upgrades*

SPS software and firmware upgrades are handled by the MCCS. Several types of upgrades and updates can be listed:

- *TPM firmware*: The firmware running on TPMs will be updated as features are added, and issues are fixed, especially during the development and commissioning phases of SPS. These updates will translate to a new firmware bitfile as well as an updated TPM driver. The TPM driver will be part of the update cycle of MCCS (described in [RD62]) whilst the new bitfile will be stored in MCCS. Version matching between the TPM driver and bitfile is assumed to be handled by the TPM driver, such that during observation configuration TM only needs to specify the firmware version.
- *LRU firmware*: Apart from TPMs, SPS is composed of additional LRUs which run firmware, such as switches. These updates are generally published by the manufacturer, and need to be

installed by a controlling entity, which in this case is MCCS. When an update is required, MCCS will place the LRU in maintenance mode (and flag any other LRUs which depend on this for correct functioning as unavailable), perform the updates through appropriate tools, run a diagnostic check to make sure that the updates were installed properly and all required LRU functionality is still available, and mark all entities as available. Version history is stored in MCCS.

- *System software*: This refers to software running onboard compute units on SPS LRUs, such as that running on the Cabinet Management board. This software can be of two types:
    - Standard operating system, where the CPU runs a light-weight operating system on which applications can be launched. The operating system itself will require updates and upgrades, which must be run whilst the LRU is in maintenance mode. The upgrade mechanism is OS-specific, but generally an update command is available in the OS itself.
    - Embedded, in which case the system and application software are combined in the same image. In this case, the LRU is updates by restarting it (and going through the appropriate state changes) and downloading the new embedded software application
- *Control software*: This refers to software running operating system in SPS LRUs and can include bespoke monitoring and control software as well as TANGO devices. This software will go through the software update cycle as defined in [RD62].

5.2.2 System Timing Synchronisation

5.2.2.1 *General Simplified Total Telescope Timing and Synchronisation*

A high-performance synchronisation distribution network is a fundamental element for the overall telescope performances. Individual samples must be labelled to the absolute time with a long-term stability of better than 1.5 ns one sigma (L3-179), while short term clock stability affects the digitisation noise and the coherence loss. A *simplified* total telescope system timing flow diagram is shown in Figure 5-4.
The SKA clock and timing structure is organised on three levels. A high stability reference clock is derived [RD63][RD73] from an atomic standard, determines the sampling accuracy. The individual samples are synchronised using a PPS signal, with a sufficiently fast edge and stability to identify the first clock edge in each second. Individual PPS edges are associated to the UTC time using NTP.

SaDT transports the clock and PPS distribution signals to LFAA cabinets, both in the CPF and in the RPFs, with predictable delay and low clock jitter. The synchronization signals come as single signals for each rack and LFAA SPS shall assure the distribution of these signals inside the SPS rack, to ADCs (for sampling) and to the SPS digital hardware (for sample time stamps).

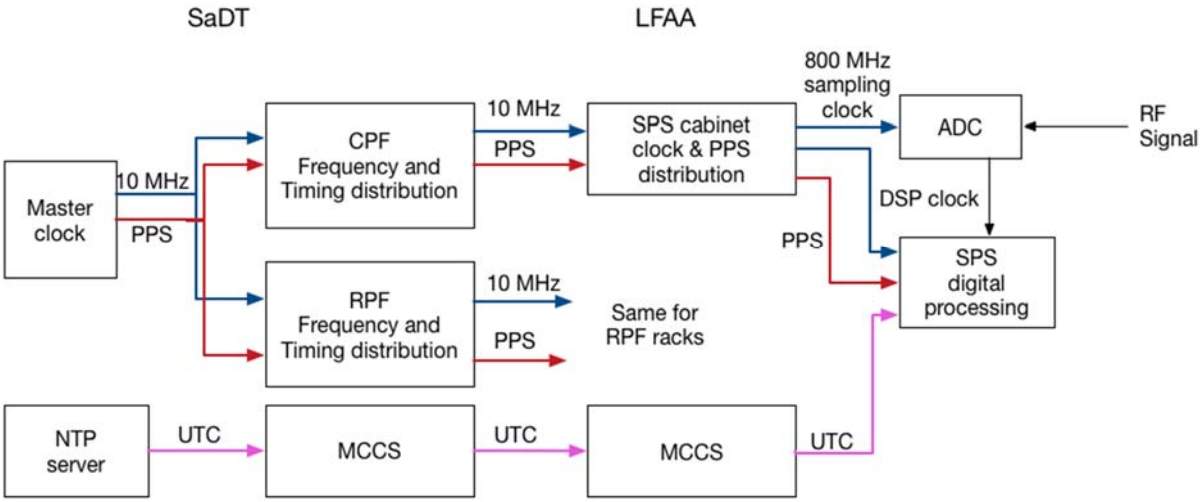


Figure 5-3 SKA Low clock and timing distribution network

5.2.2.2 *SPS synchronization*

The proposed SPS synchronisation distribution network is detailed in Figure 5-3 and Figure 5-4. Clock and time signals from SaDT will be distributed to individual boards using a three-level buffer tree [RD63]. The first level is composed by the first digital PLL, in the cabinet management board, that receives the 10 MHz tone and the PPS signal from the SaDT.

The proposed PLL, AD9545 performs two operations:

- removes the high frequency signal jitter components
- samples the PPS digital signal and inject it in the output 10 MHz as “balanced phase modulation”.

The digital PLL output is a single differential signal, connected to a x4 differential clock buffer. Each clock buffer output is filtered for the high frequency components and converted from differential to single signal with a balloon to be transmitted with a 50-ohm shielded cable to the cabinet sub-rack management boards. The signal is named 10MH+, indicating that the 1 PPS signal is embedded in the 10 MHz input reference.

The removal of the high frequency components of the 10 MHz+ generated by the cabinet management will reduce the electromagnetic emission from the cable inside the cabinet and the expected interferences related to the harmonics with the TPM optical receiver amplifiers.

Each sub-rack management board uses the same digital PLL to extract the 1PPS signal and regenerate the 10 MHz reference clock and distribute it to two passive buffers in the backplane of the sub-rack (up to three aligned differential outputs are available on the DPLL itself).

As last step, in the backplane, the two symmetrical x4 clock buffers distribute the 10 MHz reference signal to each TPM with equalised traces.

The PPS signal regenerated by the DPLL is buffered by the CPLD on the sub-rack management board and distributed on the backplane to the TPM with two x4 digital clock buffer, with single ended signals.

The proposed DPLL regenerates the output clock with a Typical RMS Jitter (12kHz – 20 MHz) of 213 fs rms and the defined distribution circuit is expected to obtain 226 fs of RMS Jitter to the TPM inputs.

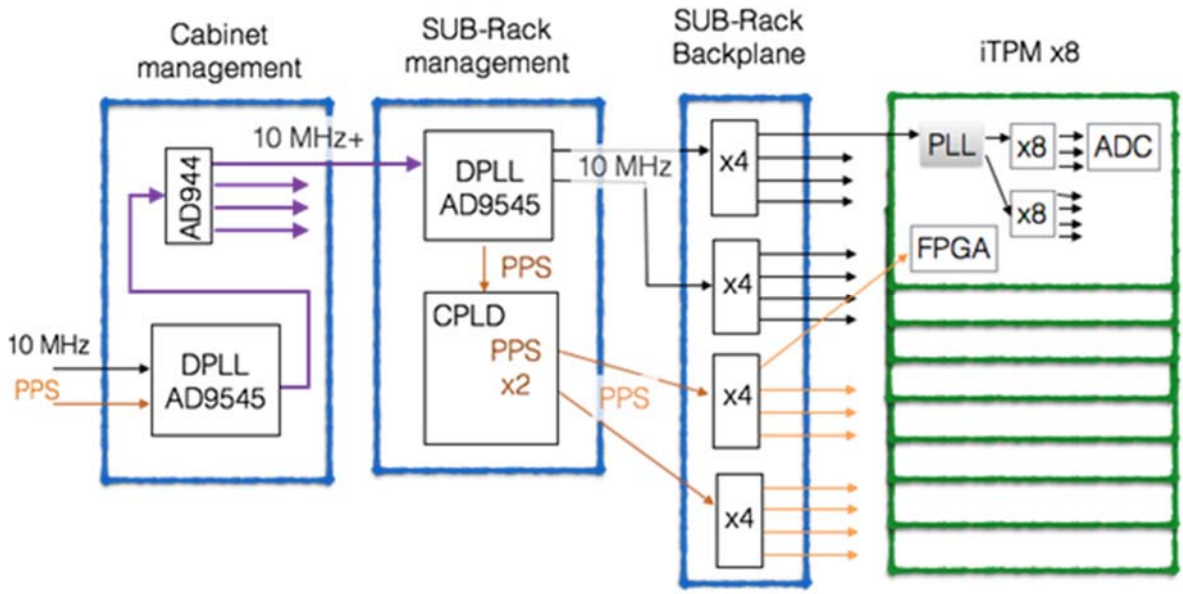


Figure 5-4 SKA LFAA cabinet clock distribution network

In each TPM the clock is then used to generate internal clock signals for sampling and for signal processing.

The PPS signal is distributed to FPGAs inside each TPM using a passive buffer tree. The signal is internally re-sampled using a locally generated 100 MHz clock, phase locked to the 10 MHz reference clock. PPS signal must be synchronised to the 10 MHz clock, with arbitrary but stable phase.

The synchronisation of multiple ADUs requires a specific procedure to set up all local clocks and guarantee a stable capture of the PPS edge. Firstly, the ADU PLL is configured to generate the required clocks. The AD9528 PLL consists of two cascaded PLLs; the first PLL controls the on-board 100 MHz VCXO and generates a 100 MHz clock which is locked to the External 10 MHz Reference clock. The generated 100 MHz clock is then forwarded to the FPGAs and used by the second PLL in AD9528 to synthesise the ADC sampling clock (800 MHz). Using the forwarded 100 MHz, the FPGAs generate locally the processing and the JESD204B transceiver clocks. JESD204B links are initialised and synchronised in a predictable way using the JESD204B Subclass 1 deterministic latency feature.

In reference to Figure 5-5, time tagging of ADC data in the FPGA is achieved using the PPS to generate an internal PPS signal that is synchronous to the processing clock and phase aligned across ADUs; being the processing clock ultimately locked to the 10 MHz Reference Clock, this signal can be used to synchronise ADUs and represents the trigger that enables the ADC data streaming from the JESD Interface towards the DSP logic. Re-sampling phase of the PPS is individually adjusted for each FPGA, during initialization, to guarantee a stable capture of the PPS edge. The PPS is sampled using the forwarded 100 MHz clock. The phase offset between a PPS edge and the following 100 MHz clock edge is measured with a resolution of 1.25 ns; the measured phase offset can be used to delay the data stream to re-align the data stream to the PPS edge.

The generated internal PPS signal can be used to increment a time counter *curr_time* which is initialised by MCCS to contain UTC time. As the internal PPS signal is synchronous across multiple ADUs, the *curr_time* counter is incremented synchronously at each PPS rising edge as well. MCCS can then initiate data streaming by writing into the register *sync_time* an UTC time set in the future. When *curr_time* assumes the same value as *sync_time*, a Start Acquisition signal is generated; this will cause the JESD Interface to start streaming data as frame of 864 samples, corresponding to 1.08 µs, from the sample identified by the PPS edge corresponding to *sync_time*. By counting the number of

streamed frames and knowing *sync_time*, each frame, and ultimately each sample in a frame, can be traced to an absolute time using the equation:

$$t_{Frame} = sync_time + 864 * time_stamp * \delta t_r$$

where δt_r is the ADC sampling period and $time_stamp$ represents the number of counted frames. If the PPS jitter, relative to the 10 MHz clock, does not exceed one sample time (1.25 ns), timing accuracy reflects that of the timing signals distributed by the SaDT.

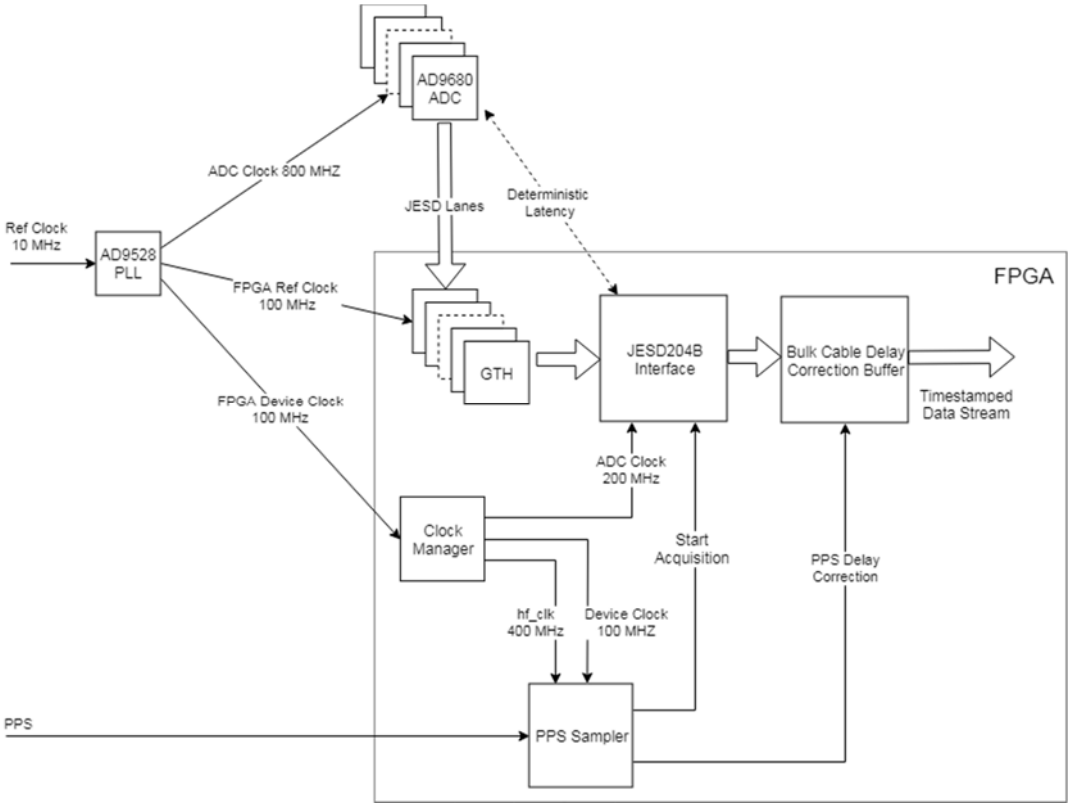


Figure 5-5 SKA LFAA ADU Synchronisation Diagram

5.2.2.3 *Clock jitter*

Sampling clock, at 800 MHz, and internal processing clock, at 200 MHz, are both phase-locked to the reference 10 MHz. Total jitter for the 10 MHz reference clock determines the jitter of the ADC sampling clock, which in turn introduces an extra noise in the system. The jitter depends in a similar way either to the RMS amplitude of a wideband signal, with centre frequency f_c and band *B*, or to the peak amplitude of a monochromatic sinusoid of frequency f_0, according to:

$$\frac{N_{sine}}{N_{adc}} = 12\left(2\pi f_0 \tau_j A\right)^2 ; \quad \frac{N_{noise}}{N_{adc}} = \left(2\pi(\sqrt{12} f_c + B)\tau_j A\right)^2$$

The two formulas are equivalent for *B=0*. The worst case for the jitter noise consists in a monochromatic signal at the highest input frequency $f_{max} = 350MHz$. Assuming the tone has a peak amplitude *A* of 100 ADC units, the added noise relative to the ADC quantization noise is given by:

$$\frac{N_j}{N_{adc}} = 12\left(2\pi f_{max} \tau_j A\right)^2 = \left(\frac{\tau_j}{1.3ps}\right)^2$$

A jitter of 400 fs would contribute an extra noise of about 10% of the ADC quantization noise, or 0.1% of total added noise. It should be noted that such a large RFI level, if modulated and not a pure tone, would cause severe clipping and generate harmonics. Maximum safe level for RFI is around 1/3 of the clipping level RMS, or about 60 ADC units peak, with corresponding higher jitter (about 750 fs RMS). Current jitter specification has been assumed to be 400 fs at the ADC sampler, divided (quadratically) as 280 fs in the SaDT and 280 fs in the LFAA clock distribution tree.
Jitter spectrum is also important, as the low frequency jitter noise contaminates mainly the portion of the spectrum close to the offending RFI signal. The wideband jitter is mainly due to the PLL generating the ADC clock, while the corresponding incoming jitter is filter in the PLL loop. Low frequency jitter is dominated by the corresponding jitter in the clock distribution chain.
The PLL used in the TPM is the AD9528, that has a noise floor of -161 dBc at an offset greater than 10 MHz This corresponds, over an 800 MHz band, to a jitter of 30 fs. Total jitter in the SPS distribution tree is around 220 fs.

5.3 SPS Top-Level Static Decomposition

Figure 5-6 shows the top-level static decomposition of SPS, with Level 3 (SPS 163-000000) Level 4 (163-010000 for the populated SPS Cabinet and 163-020000 for the SPS Network Infrastructure) and Level 5 SKAO PBS components:

- TPM Sub-rack 163-010001
- AC power distribution 163-010002
- Cooling system 163-010003
- Cabling 163-010004
- 100 G Ethernet Switch 32 ports_1 163-010005
- 100 G Ethernet Switch 32 ports_2 163-010006
- Cabinet Management board 163-010007
- Cabinet Management board software 163-010008
- Cabinet chassis 163-010009
- Cabinet 1 G switch 163-010010
- RF over Fibre cable assembly 163-010011
- LFAA SPS to CSP high speed data cable 163-010012
- DDBH equipment CPF 163-020001
- SPS to DDBH high speed data cable 163-020002
- RF over Fibre patch cabinet 163-020003
- DDBH equipment in the RPF 163-020004

Lower level items are identified in the SPS PBS contained in the Construction Costing spreadsheet [RD54].

5.3.1 SPS Top-Level Static Decomposition Diagram

The SPS cabinet is the main component of the SPS. Identical cabinets are used in the core and remote stations, with each cabinet implementing the SPS functionality for two stations. Data network equipment component groups all elements that are not modular to a cabinet.

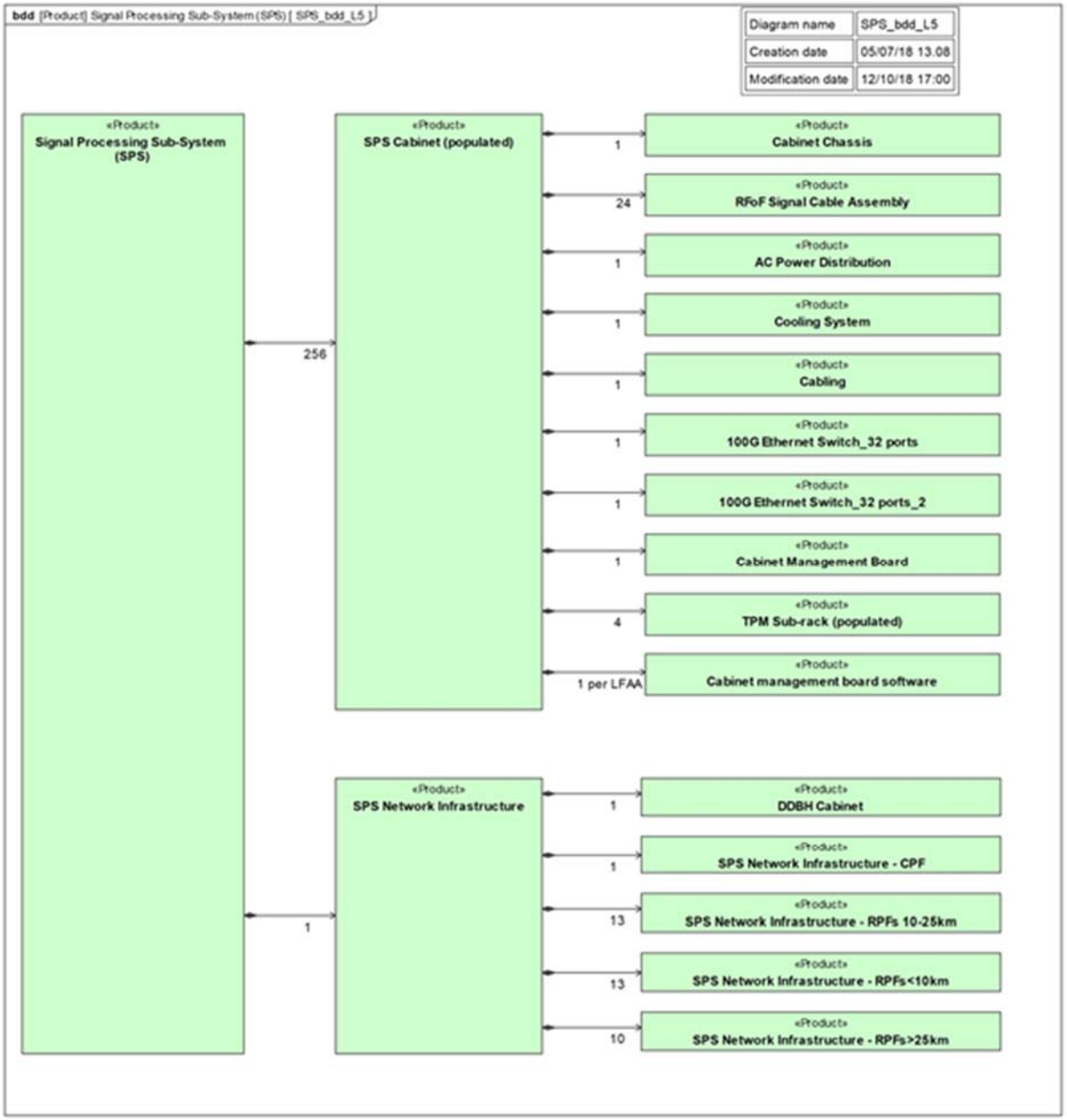


Figure 5-6 SPS Top-level Static Decomposition

5.3.2 External Entities

There are no external entities in the SPS static decomposition diagram. Verification and maintenance support equipment is not described in detail in this DDD.

5.3.3 Level 4 and 5 Components

Level 4 decomposition has only two elements:

- 256 identical SPS cabinets, each one providing SPS functionality for two stations
- Signal and data network equipment not related to a single SPS cabinet. This mainly includes equipment related to data transport in remote stations (long haul link drivers) and the optical link splice cabinet that interfaces to the field node fibres.

SPS cabinet is composed of:

- The cabinet chassis, holding all other components
- Two 40/100 Gbps 32 port switches, implementing a single 40/100 Gbps Ethernet network for science data
- The Cabinet Management Board (CMB). This implements also a 1Gbps Ethernet switch, for the control and management network
- The AC power distribution system, distributing AC power to all Level 4 components under CMB control
- The Cooling System, to remove heat from other level 4 components
- Four TPM sub-racks, processing signals from 128 antennas each
- The RFoF cable carrying the antenna signals from the splicing cabinet
- Required internal cabling.

Cabinets hosted in the CPF and those in RPFs are identical. RPF cabinets physically host the long-haul drivers and associated equipment, belonging to the SPS network sub-element.
Internal static decomposition of one SPS cabinet is shown in Figure 5-7. LRUs are shown in blue if repairable, and yellow if not repairable, and include:

- All rack mounted items. The TPM sub-racks contain LRU boards, but can be replaced as a complete unit, after removing the LRU boards.
- Cooling main unit (liquid-to-liquid) and associated sub-elements, contained in a standard rack mounted cabinet.
- Liquid-to-air heat exchanger mounted on the side space of the cabinet
- All electric power distribution elements mounted on DIN rails
- All cabling
- Water pipes and valves

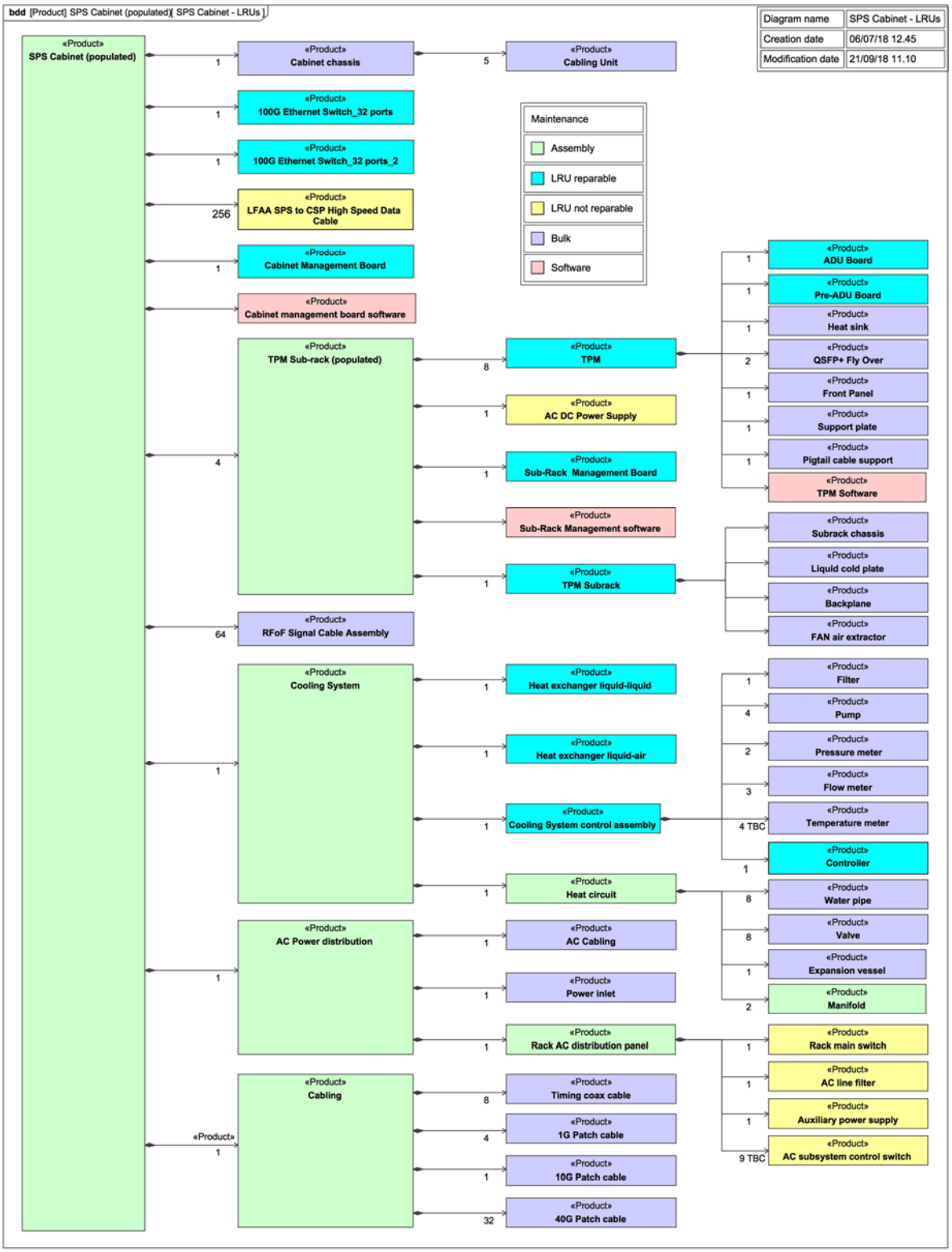


Figure 5-7 SPS Cabinet Static Decomposition with highlighted LRUs

5.3.4 External Interfaces

External Entity	Interface Control Document & Interface ID	Leading Organization	Key Data or Message flows and Applicable Requirements
CSP	100-000000-004 S1L-LFAA-CSP-001	LFAA	Beamformed data packets
INAU	100-000000-003 S1L-LFAA-INAU-004	LFAA	Routing of RFoF breakout cables to cabinets
INAU	100-000000-003 S1L-LFAA-INAU-005	LFAA	SPS Cabinet power
INAU	100-000000-003 S1L-LFAA-INAU-006 S1L-LFAA-INAU-007	LFAA	Routing of 10 MHz and 1PPS cables to SPS cabinets
INAU	100-000000-003 S1L-LFAA-INAU-008	LFAA	SPS Cabinet Cooling Fluid
INAU	100-000000-003 S1L-LFAA-INAU-009	LFAA	SPS Cabinet and Splice Cabinet floor space and shielding
SaDT	100-000000-026 S1L-SaDT-LFAA-001 S1L-SaDT-LFAA-002	SaDT	10 MHz and 1PPS signal distribution to SPS cabinets (CPF)
SaDT	100-000000-026 S1L-SaDT-LFAA-003 S1L-SaDT-LFAA-004	SaDT	10 MHz and 1PPS signal distribution to SPS cabinets (RPF)
SaDT	100-000000-026 S1L-SaDT-LFAA-007	SaDT	CPF interface to long haul cables Beamformed data packets (to CSP) Transient buffer data and LMC (to MCCS)
SaDT	100-000000-026 S1L-SaDT-LFAA-008	SaDT	RPF interface to long haul cables Beamformed data packets (to CSP) Transient buffer data and LMC (to MCCS)

L2 interface to other LFAA Sub-elements are shown in Figure 5-8.

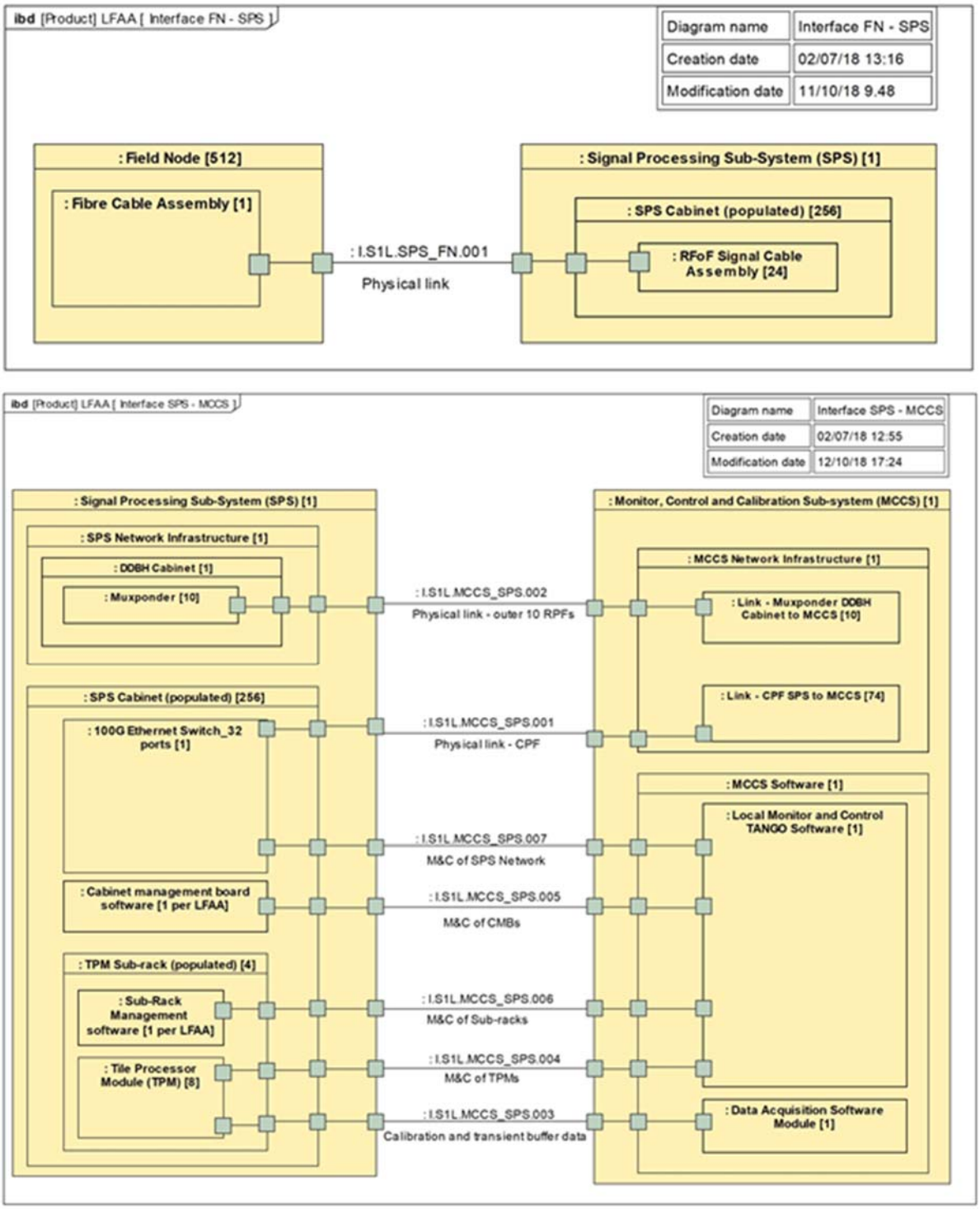


Figure 5-8 LFAA Internal Interface Diagram Showing Interfaces between Level 3 Components

5.3.5 Internal Interfaces

LFAA Entity	Interface ID	Key Data or Message flows
FN	S1L_SPS_FN-001	RFoF radio signal, FN monitor and control (physical layer only)
MCCS	S1L_MCCS_SPS-001	Mechanical-optical interface between CPF cabinets and MCCS
MCCS	S1L_MCCS_SPS-002	Mechanical-optical interface between long haul switches and MCCS
MCCS	S1L_MCCS_SPS-003	Calibration, Transient Buffer and LMC data
MCCS	S1L_MCCS_SPS-004	TPM monitor and control
MCCS	S1L_MCCS_SPS-005	Cabinet Management Board monitor and control
MCCS	S1L_MCCS_SPS-006	Subrack management board monitor and control
MCCS	S1L_MCCS_SPS-007	Network switches monitor and control

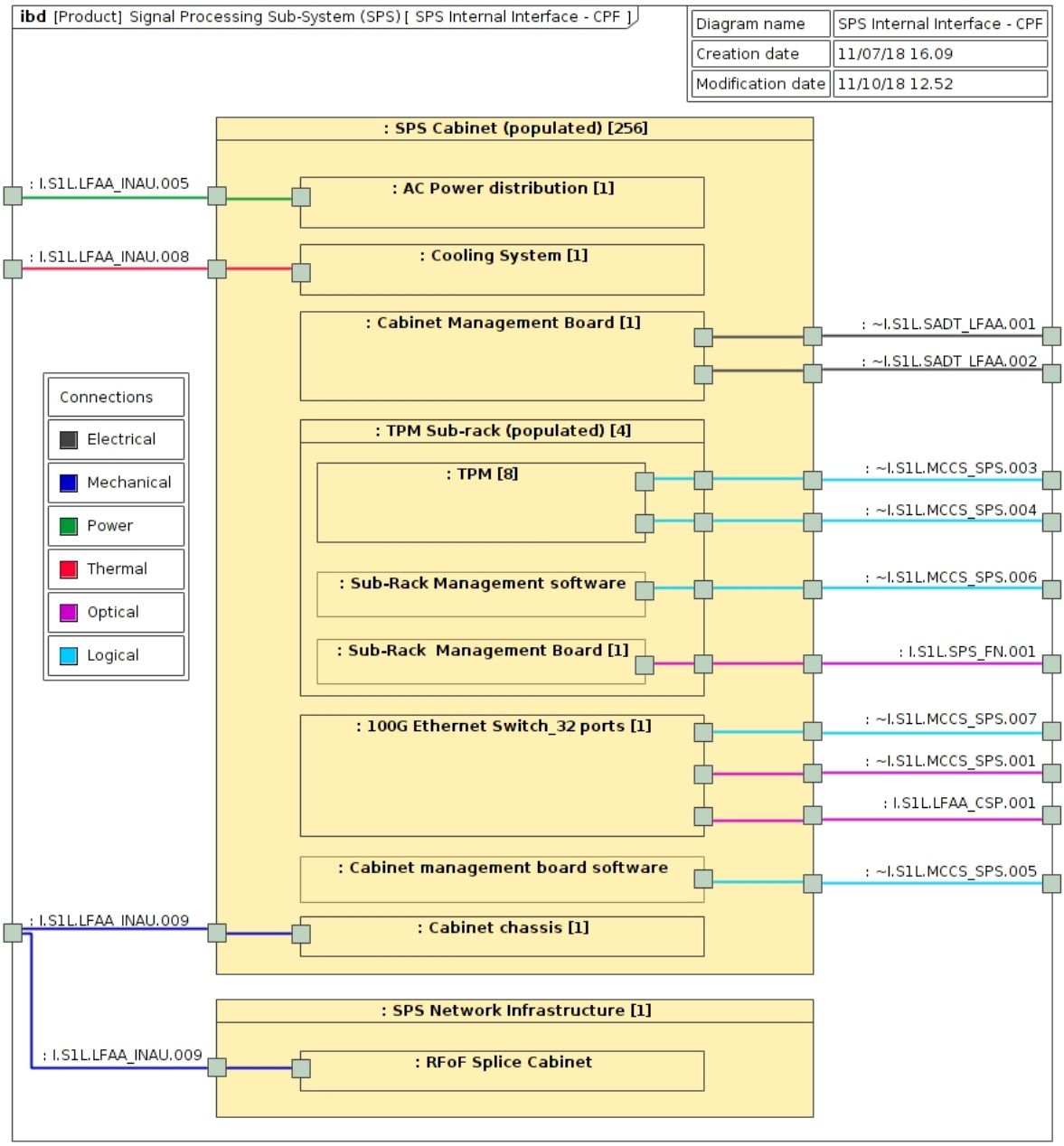


Figure 5-9 SPS Internal Interface Diagram Showing Interfaces between Level 4 Components (CPF racks)

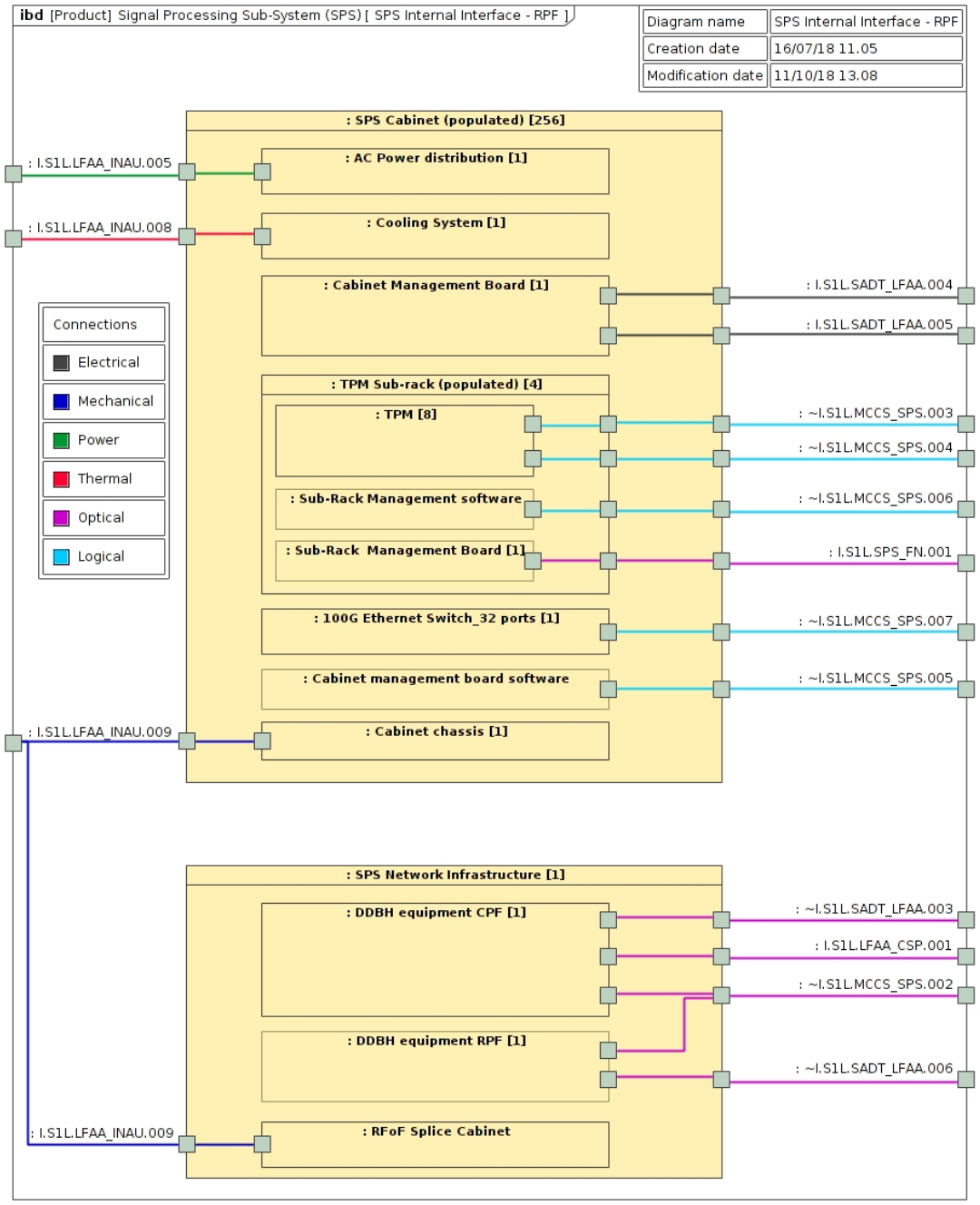


Figure 5-10 SPS Internal Interface Diagram Showing Interfaces between Level 4 Components (RPF racks)

5.4 Hardware and Mechanical Components

5.4.1 Tile Processing Module

The TPM is one of the most complex assemblies used as an LFAA LRU component and it is the main processing component within the SKA-LFAA element. It is a hybrid analogue/digital module that receives 32 analogue input signals coming from 16 dual polarization antennas (one SKA tile) via RFoF links and contributes with the cooperation of other tile processors to form the station beam. In fact, since each TPM computes the beam of one tile and sums the incoming partial beam from previous tile

processors with the tile beam formed locally, when connecting more tile processors in a daisy chain the output of the last will be the beam of the station.
For a complete description of the relevant functionality of TPM please refer to [RD14]

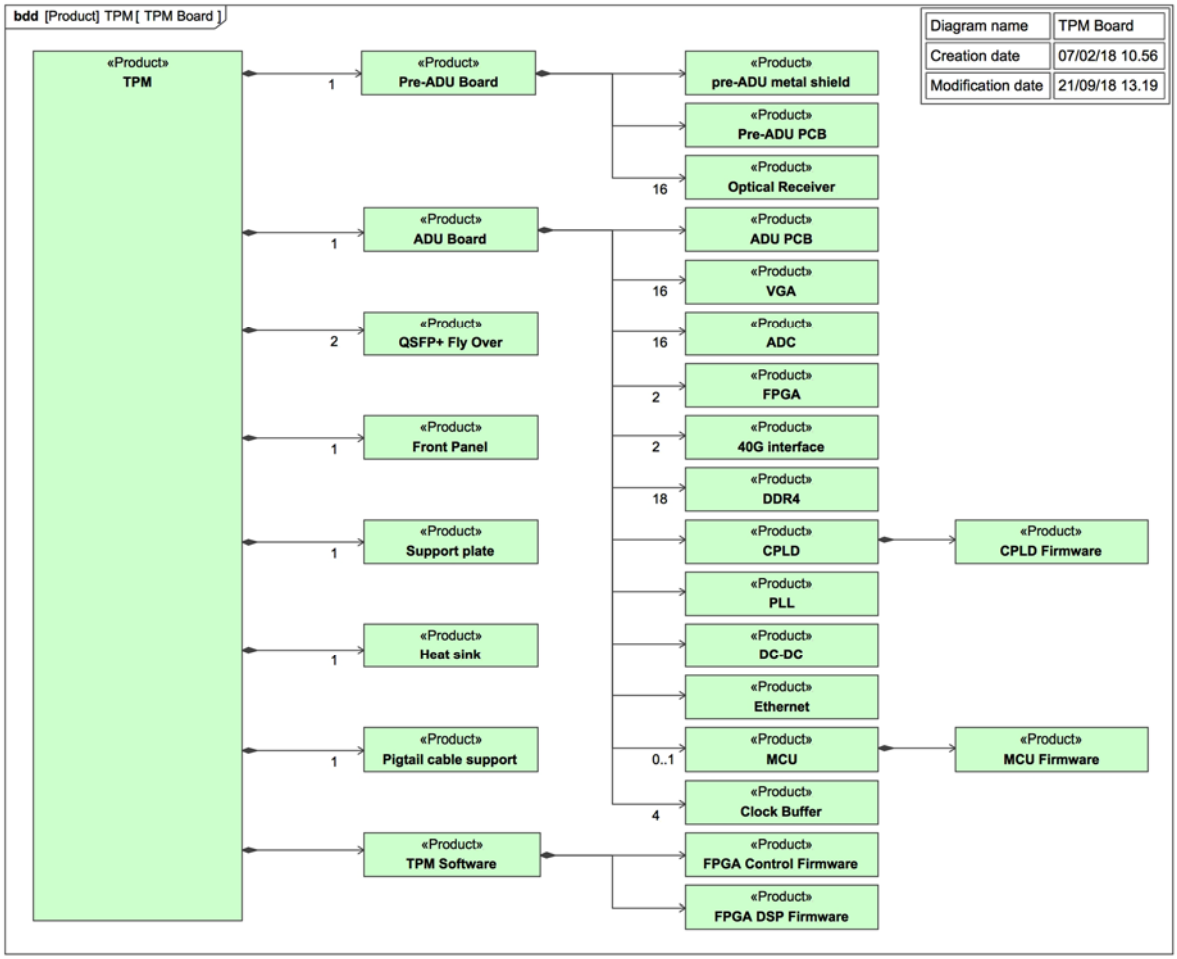


Figure 5-11 TPM 1.5 Static Decomposition Diagram

The static decomposition diagram for the TPM is shown in Figure 5-11. The TPM is mainly composed of two boards: the pre-ADU boards that are devoted to optical-electrical conversion, filtering, amplification and equalization of 32 analogue signals, and the ADU (Analogue to Digital Unit) board, which has the task of: analogue to digital conversion, polyphase filtering, application of calibration and beamforming coefficients, sum of all 32 signals to form the tile beam (local), sum the tile beam with the incoming partial station beam and transmission of the data to the network (switch). The two boards are supported by a metal plate and cooled using a heat sink employing heat pipes.
Several generations of the boards which form parts of TPM assembly have been generated and produced to verify the performances, the effectiveness of architecture but also used to develop the FW/SW necessary for FPGA and the microcontroller on board.
The work in AAVS-1 has been to de-risk this development as much as possible and optimise the design with industry participation. The version mentioned is the TPM 1.2 (assembly of ADU1.2 & pre-ADU 2.1) For details refer to the document [RD53].

A more integrated version has been designed for LFAA to be delivered for CDR (TPM 1.5) by INAF/Oxford in collaboration with Leonardo Finmeccanica, Sanitas EG and AAVID Thermalloy. The process of optimisation has not finished yet and fine tuning of the design is still in progress and will continue during the bridging phase.

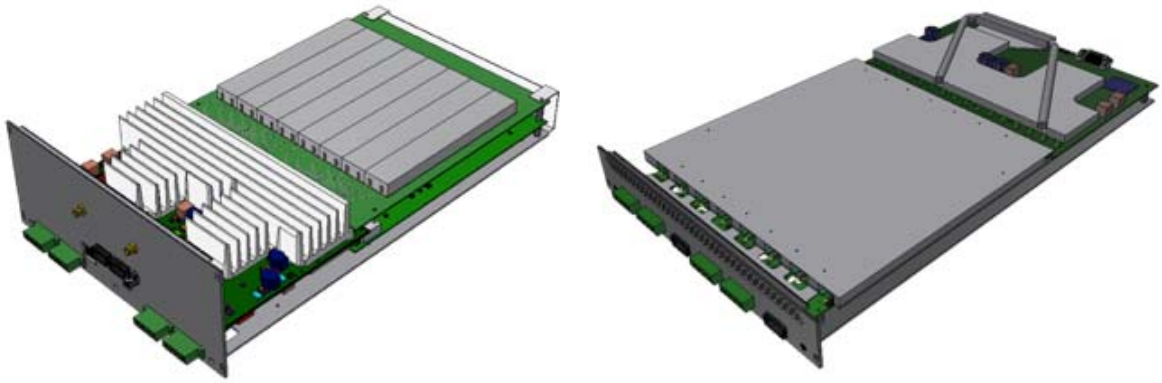


Figure 5-12 TPM 1.2 (AAVS1) vs TPM 1.5 (LFAA): From the design is possible to see the difference (in term of integration) of the two assemblies

5.4.1.1 *Pre-ADU Board*

The Pre-ADU board corresponds to the analogue receiver in front of the ADU. The current design pre-ADU 2.1 hosts 16 double channel analogue receivers (i.e. 32 analogue chains). The two chains in each double channel receiver correspond to the two antenna polarizations.
The first stage of any Pre-ADU channel is an optical receiver (ORX) which converts back to the RF domain the signal transmitted through an optical fibre from the remote antenna. The current Pre-ADU version adopts WDM (Wavelength Division Multiplex) optical receivers, which paired with WDM optical RFoF (RF over fibre) transmitters at the antennas, allow to use one single fibre for both antenna polarisations.
A standard direct RF receiver (i.e. without any frequency conversion) follows the ORX. Several functions are here included to adapt the signal for the digital conversion: amplification, level adjustment (by means of a digital step attenuator, 31 dB range/1 dB step). The digital step attenuator is controlled by ADU board via the SPI bus.

The architecture of the pre-ADU board is reported in [RD65].

The design of this board is still progressing simplifying the mechanics and interconnection to ADU, but also the RF electronics. In particular, we would underline that the future generation will consider the possibility to use a differential driver stage in front of ADC (what we called VGA) and thus, it will allow us to avoid the last amplification stage and any digital control on board because the VGA is directly controlled by SPI.

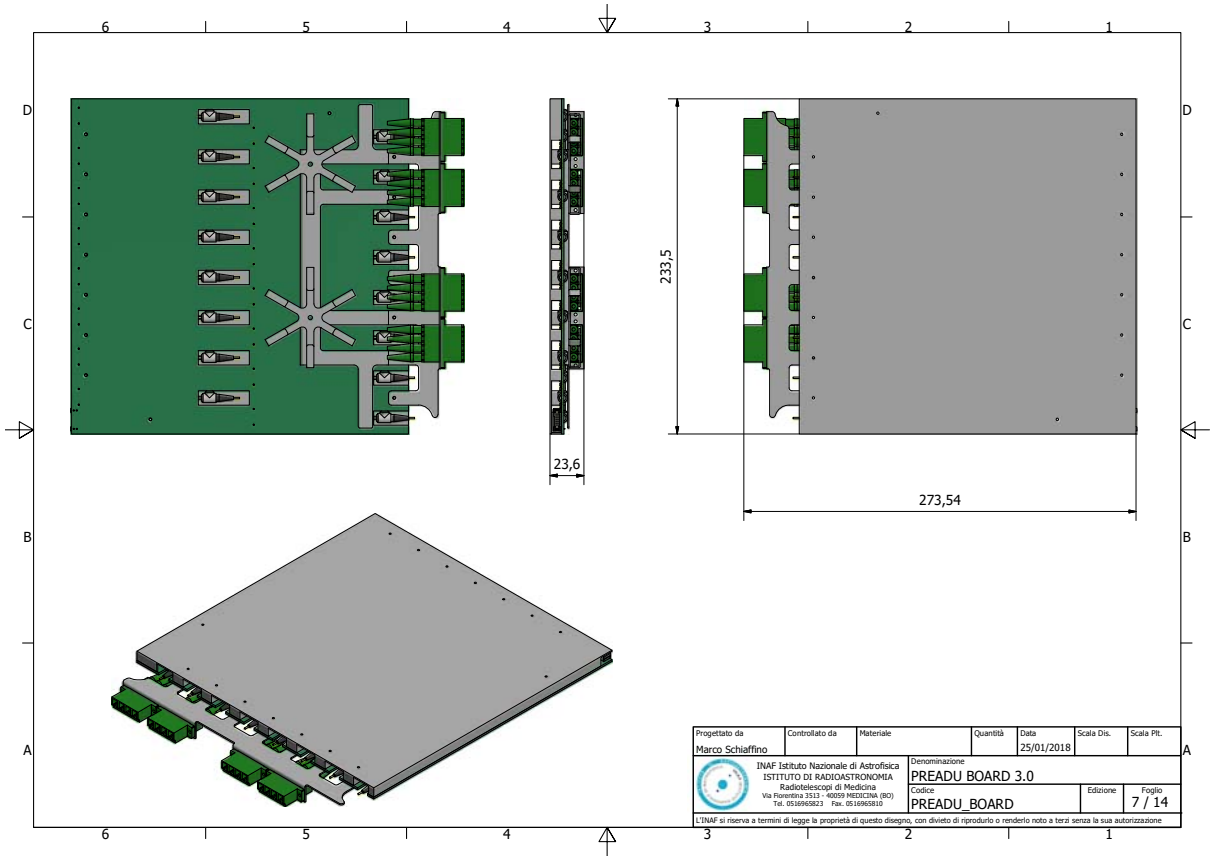


Figure 5-13 Image of prototype Pre-ADU board

5.4.1.2 *ADU-Board*

The ADU is the Tile Processor Board of the Square Kilometre Array. It is a 32 channel 1 GHz Analogue to Digital conversion/pre-processing board, equipped with management functions to support the integration into the rack structure.
Best in class 14-bit AD converter, latest 20 nm FPGA, 40 Gbit Ethernet optical link have been selected focusing on the best commercial compromise between quality, performance and power consumption. Compact board size, low noise clock network, advanced 14-layer board build-up, complete Ethernet based management features (including health monitoring capability), high efficiency and low noise power distribution system complete the main board features.
The TPM provides also external synchronisation signals and high speed DDR4 memory banks to allow RAW data buffering.
An on board 32-bit microprocessor and large flash memories allow high-level management operations including on line multiple configuration selection and structured communication with infrastructure management applications.
The TPM board is provided with low-level management firmware to perform board configuration and monitoring through the Ethernet interface exploiting a UDP based protocol.
The following list sums up the principal TPM characteristics and features:

- Compact size, 6U format compatible
- Thirty-two analogue input capability with high quality and high isolation stackable RF 50 Ohm input connectors
- Sixteen dual channel analogue programmable drivers (amplifier/attenuator)
- Sixteen dual channel 14 bit 1GHz AD converters

- High quality clock distribution system with full JESD204B Subclass 1 capability on all inputs, with deterministic latency between the channels and the user configurable low noise PLL
- Two Xilinx Ultrascale+ XCKU9P 16 nm FPGA devices dedicated to data processing, pin to pin compatible, implementing the same functionality
- Two DDR4, 64-bit memory banks, up to 16 G Byte total size
- Two 40G Ethernet interfaces (QSFP), one for each FPGA
- High speed internal bus to connect the 2 FPGAs, 40 Gbit + 40 Gbit bidirectional
- Low-level Ethernet gigabit management interface with instant ON flash-based Lattice CPLD
- Complete system monitor interface with power, voltage and temperature monitoring
- On board two 256Mbit SPI user flash for multiple FPGA configuration options
- Second level management Microcontroller Unit (ARM Cortex M4, 32-bit, 120 MHz) for high level remote board control
- High efficiency multistage Power Distribution system, with configurable start up sequence and selective function related power control capability.

The board is logically divided in the analogue to digital chains very close to the pre-ADU connectors (only 15% of the PCB surface area) and the digital part which hosts devices for processing data, management, DC-DC power supplies and input/output interfaces.
Each FPGA manages 16 data streams (one polarization each) connected via JESD204B links, performs the signal processing and transmits the output using Ethernet UDP packets.

More details about the requirements and the design of the signal processing architecture of the ADU board can be found in [RD64].

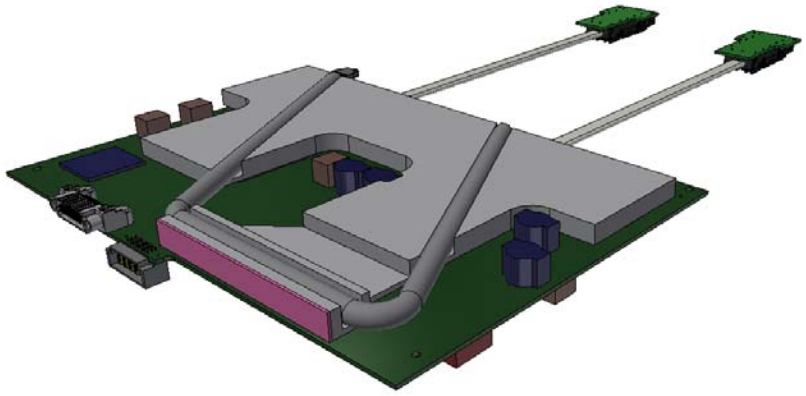


Figure 5-14 Image of prototype ADU board

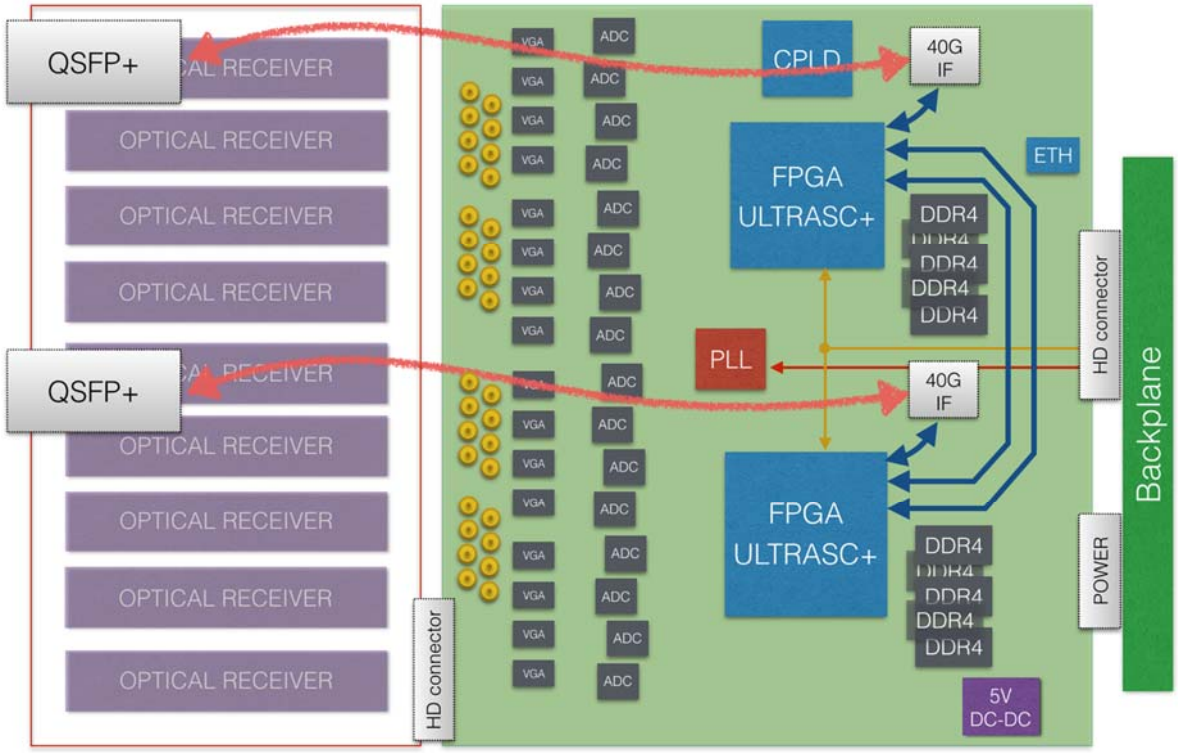


Figure 5-15 Board Layout of Major Components

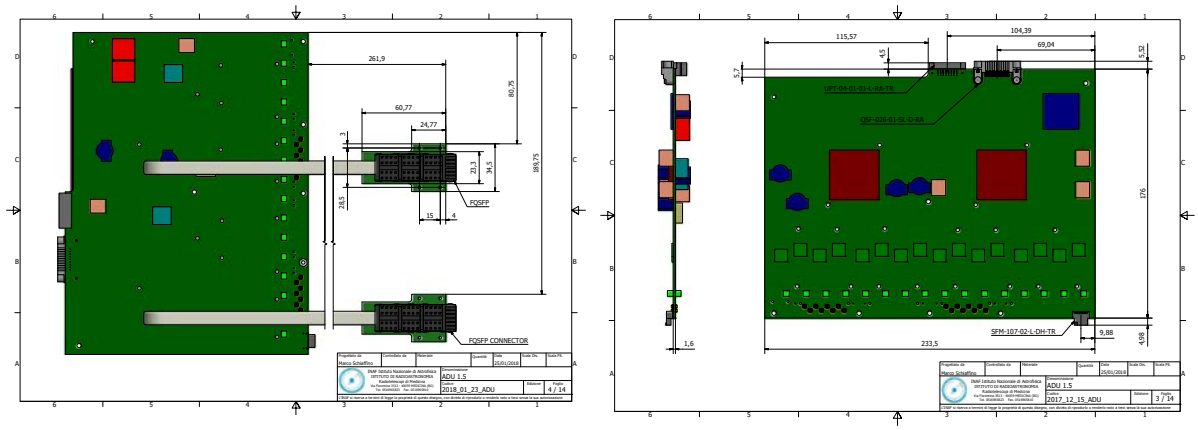


Figure 5-16 ADU Board Top Level Schematic

5.4.2 Cabinet Management Board

The Cabinet management is structured over three levels: cabinet level, sub-rack level and TPM level. The management functions related to a specific level shall be allocated to a corresponding element to allow proper functional separation and maintainability.

Cabinet level functions include power distribution, cooling and other electromechanical interfaces. The CMB interfaces to the power distribution and cooling system to delegate the respective functionalities but is seen as a single entity from the Management and Control system.

Sub-rack level functions include: sub-rack level power distribution (to TPMs), TPM configuration, TPM start-up sequence, synchronization distribution, cooling and status monitoring.

TPM level functions execute the power management and configuration commands and support the TPM system monitoring for internal voltages and temperatures.

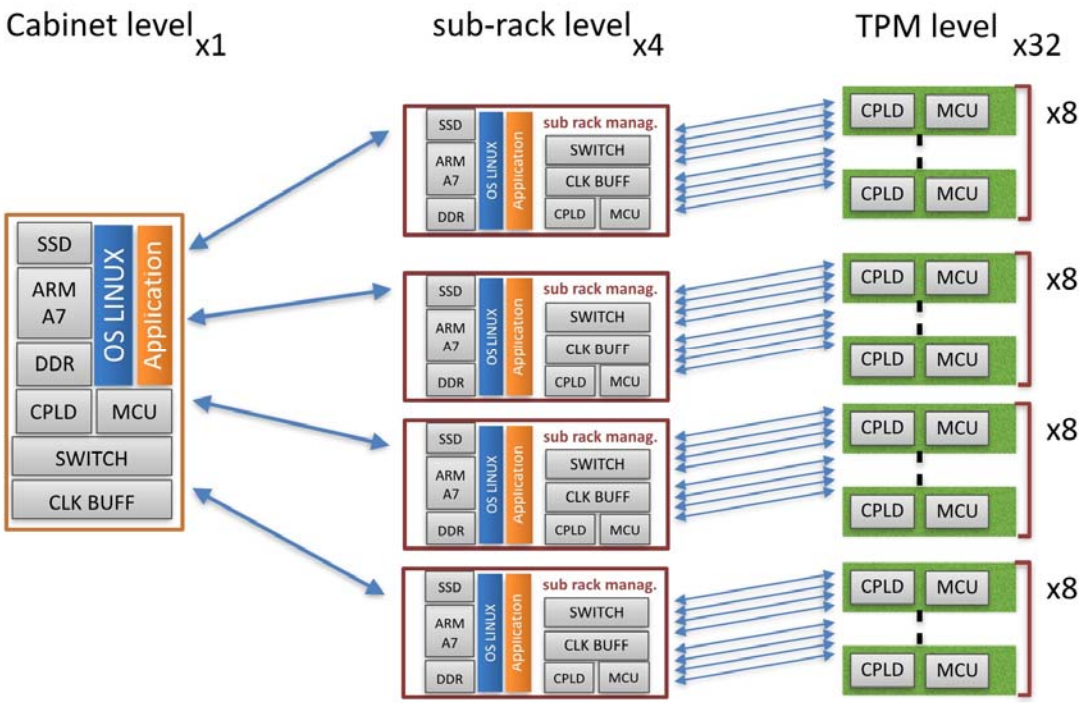


Figure 5-17 Cabinet management processing architecture

Each level communicates with a dedicated Ethernet gigabit connection with UDP based protocol for direct memory access and TCP protocol (or similar) for high level operations.
At cabinet and sub-rack levels a complex CPU, with Linux OS is present to manage secure TCP based communication with the Telescope Manager and the MCCS applications. The CPUs is directly connected on the gigabit network. Each board provides a CPLD with a hardwired gigabit UDP interface to allow the low-level hardware direct interface and safety critical functions to avoid the need of a real time OS on the CPU.
On the TPM a simple MCU integrate the CPLD functions to execute sequential operations and complex commands received from the management software.
The SPS Management Board integrates the TPM service functions required at Rack and Sub_Rack level with Hi-Level command interface with the telescope manager application.
The Management board is instantiated in two possible configurations, Rack and Sub_Rack with combined functions.
In the Rack configuration the Management board is boxed in a 1U drawer to provide the following main functions:

- Interfaces with the SKA 40G Ethernet network
- Provides the Rack level 1G local Ethernet Network
- Interfaces with the SKA 10 MHz & PPS Rack synchronization signals and distribute them in the Rack
- Provides a Linux-based CPU to execute high level Rack function
- Interfaces all rack elements for remote control operation and monitoring

The following list sums up the principal Management Board characteristics and features:

- 6U size format compatible, 350 mm depth
- Single supply, 12 to 24V DC input
- 1x4 High Quality passive 10Mhz clock distribution (differential)
- 1x4 PPS distribution (single ended)
- Digital PLL High Quality 10 MHz re-generation and PPS encoding/decoding

- One 40G Ethernet interfaces (QSFP) with only one 10G Ethernet active
- Up to 18 port Ethernet Gigabit Switch with 10G Uplink
- Low-level Ethernet gigabit management interface with instant ON flash-based Lattice CPLD
- High performance CPU ARM9 based, dual core running @ 1Ghz with enhanced capabilities
- Solid state 4GByte FLASH system memory, for OS and data
- Four DDR3L, 64-bit memory banks, 1 G Byte total size running @ 1 GHz
- SD card slot for FLASH memory expansion
- Two USB 2.0 and HDMI output for additional User Interface
- CPU trace port available on a high-speed connector for SW debugging
- Complete system monitor MCU with power, voltage and temperature monitoring
- 256Mbit SPI user FLASH
- Two I2C board temperature sensor
- Two EEprom for board configuration data with pre-assigned MAC address
- Expansion GPIO connector with UART, CAN, SPI, I2C, PWM available functions
- SATA II interface connector for hard disk storage capabilities
- PCI Express 1x interface for expansion capabilities

The Management board fits a 6U high and 350 mm depth rack mount format, compatible with next TPM 2.0 defined layout.
The Rack configuration connectors are grouped on the front side, the Sub_Rack ones are on the two lateral sides.
A preliminary overview of the board mechanical layout top view is available in Figure 5-18

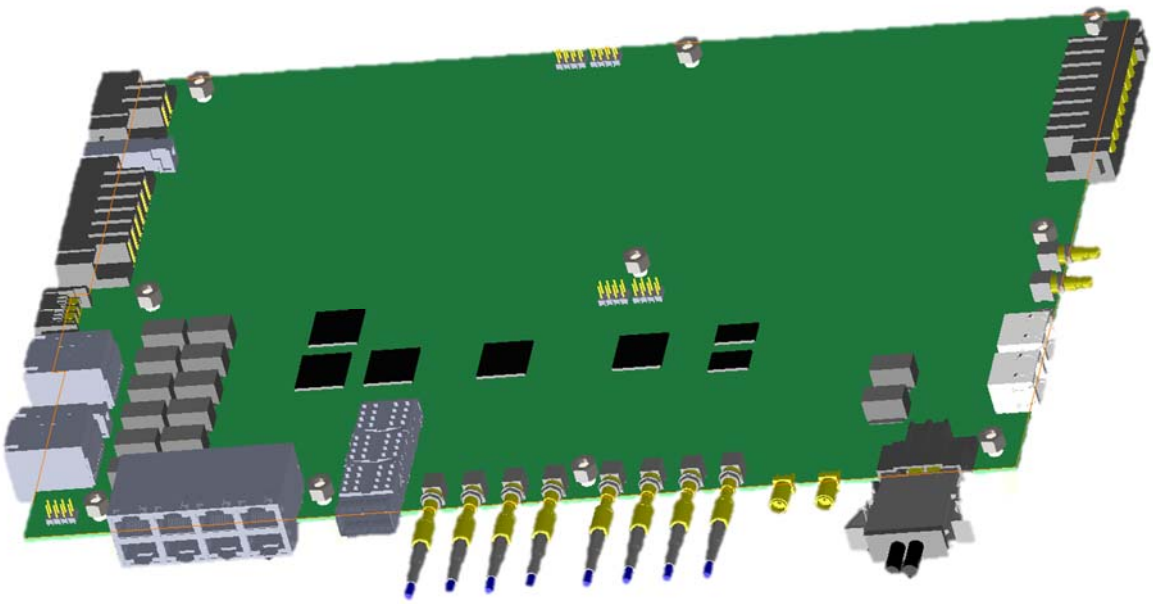


Figure 5-18 Management TOP preliminary mechanical layout

In the “Backplane” side of the board, on the Left in the image, scalable configuration is provided for a x8 TPM Sub_Rack configuration. The three connectors in the center of the side are required for both configurations.

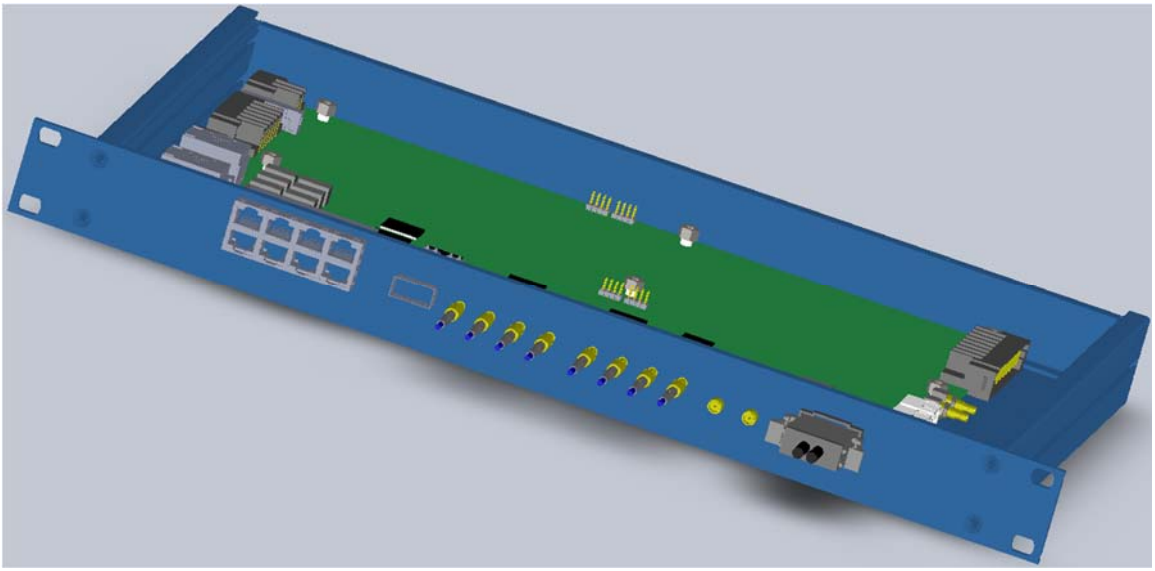


Figure 5-19 Rack configuration

The board is designed to avoid active dissipation in a controlled temperature environment. In the 1U drawer and in the Backplane a low speed air circulation shall be enough for heat sink dissipation. In the bottom side only, low profile components are present without significant power consumption.
Board Layout is organised with function specialised areas for optimal layout and performance.
The clock areas are considered RF circuit and separated from the possibly noise sources high speed digital circuits, with the same approach successfully adopted on the TPM board.

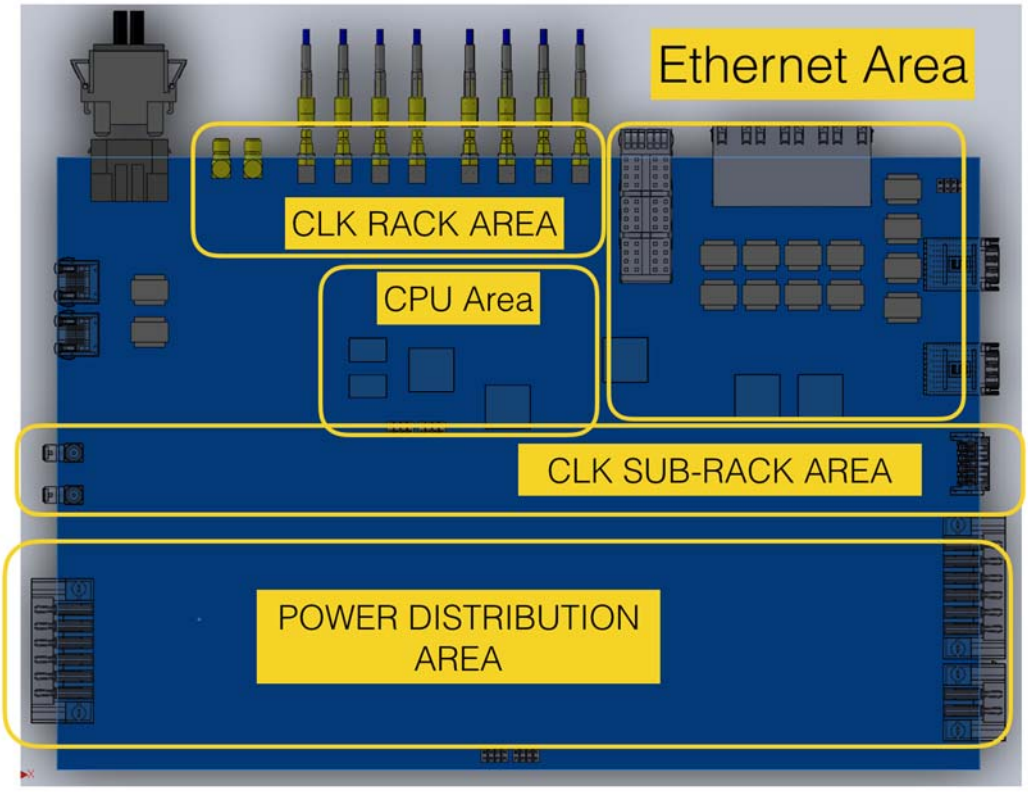


Figure 5-20 TOP placement and Layout guidelines

The overall generous board size (233x350 mm) allows optimal placement and component separation, for dissipation and isolation issues.
For the clock layout, the bottom side will be preferred for all the RF critical devices.
All the digital circuits, excluding some low power memories, are placed on the top side to simplify the board assembly and testing.
Detailed description of functions allocated to the Cabinet management board are available in [RD66].

5.4.3 SPS Network

The SPS network is an appreciable and integral part of the overall LFAA communications network as illustrated in Figure 5-21.

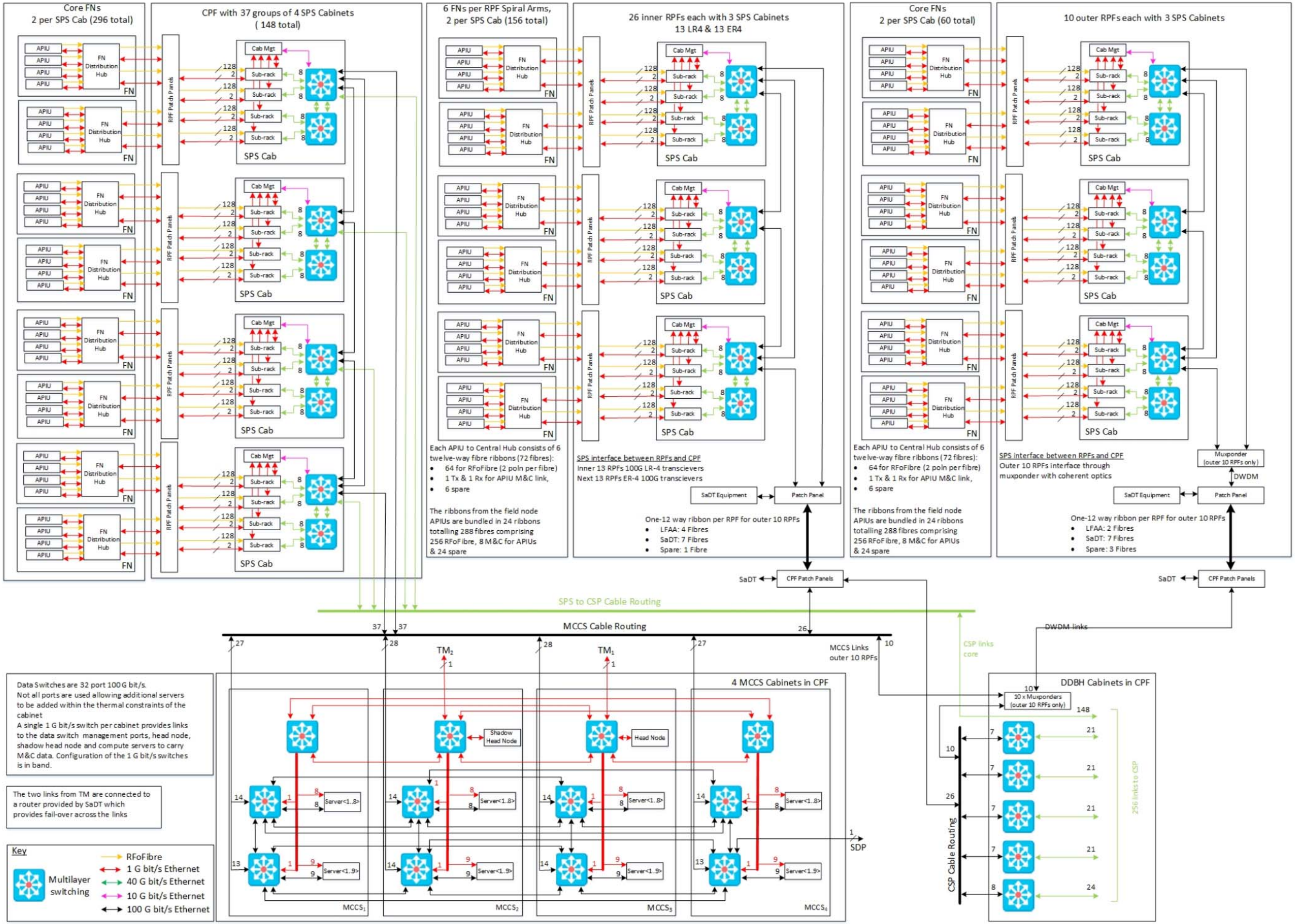


Figure 5-21 LFAA Network

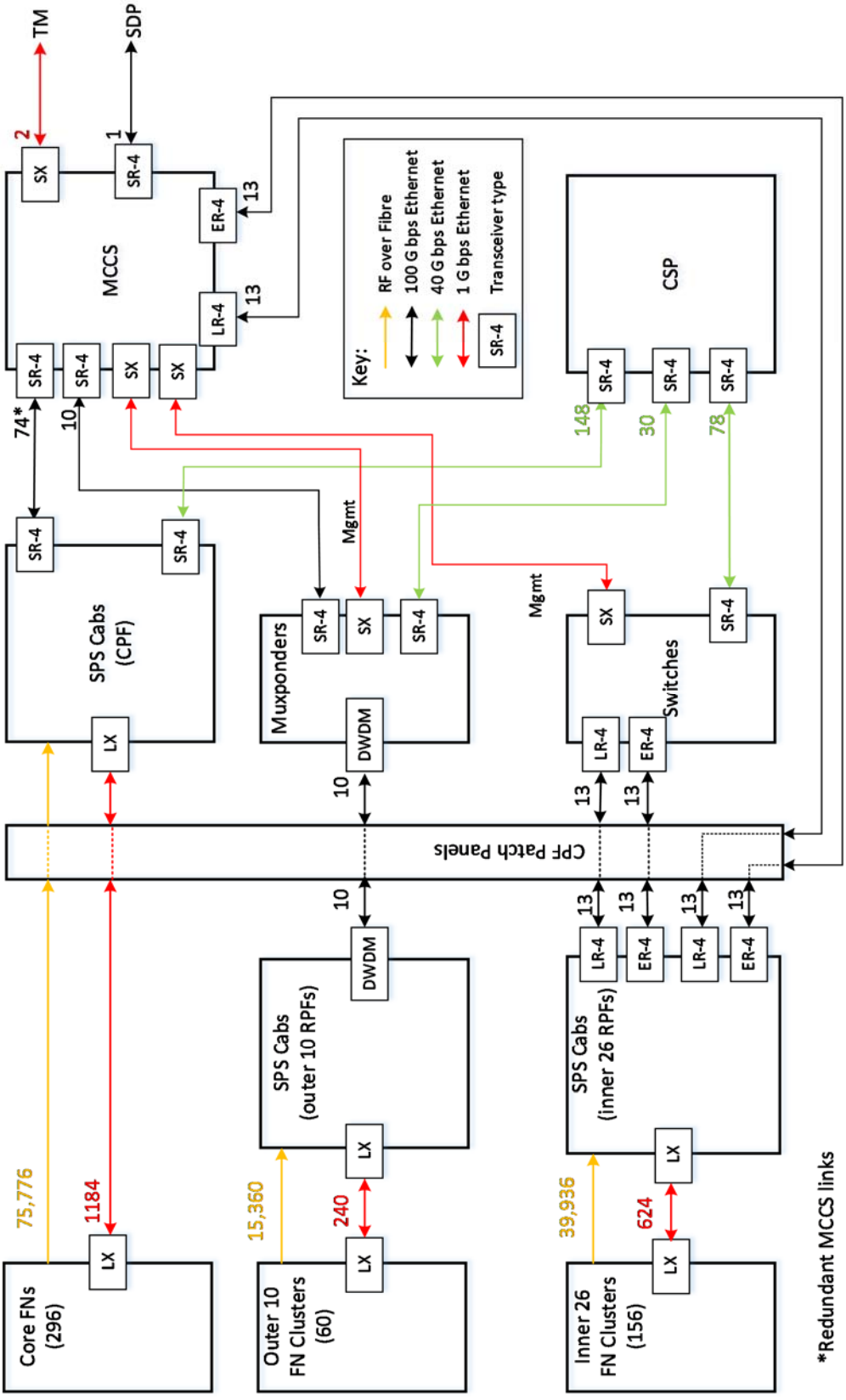


Figure 5-22 Top level network diagram identifying transceiver types

The LFAA network utilises multilayer Ethernet switching and connectivity to facilitate the data flows primarily within and between the SPS and MCCS sub-Elements. This is mostly based on commercially available equipment such as 19" rackmount switches. However, in some cases, such as the TPM, this is supplemented by bespoke design to support Ethernet connectivity in association with FPGA processing.

The LFAA network is multilayer configured for routing on the main data switches and Layer 2 for the Cabinet monitor and Sub-rack connectivity. Data flows at network Layer 2 are mostly in parallel with little need or no need for cross-connections or redundant communication paths. However, for the main cabinet data switches there is a ring topology for subsets of the network to ensure maximal use of the 100 G bit/s Ethernet capability whilst minimizing the number of transceivers and cable interconnects. Although a ring topology introduces extra communication latency in terms of the number of switch hops, this is not considered an issue. Within the core, interconnection is across 4 cabinets i.e. 8 switches whereas the interconnections in the RPFs are across 3 cabinets i.e. 6 switches. The group size allows ~ 50 to 60 percent loading of the 100 G bit/s links which minimises cabling but also keeps the probability of data collisions at switch egress ports low. Where data flows merge at an egress port, the instantaneous bandwidth can potentially exceed that of the port even is the average data rate is compliant. The switch will typically offer a configurable amount of memory buffer at the egress point but if this is exceeded packets will be dropped. Constraining bandwidth and keeping data flows even as a function of time avoids this problem and the need for tuning memory buffers on the egress ports. For this reason, the TPMs ensure beam and calibration products are delivered across the network with a smooth bandwidth as a function of time.
Assuming IPv4 addressing, SPS data connectivity will be grouped into private class C sub-nets of the 8 stations within 4 cabinets. This corresponds to the order of 150 IP addresses (mainly those for the TPMs and Sub-rack management) within the total of 254 available for the sub-net. The management nodes within the APIUs of the corresponding Field Nodes will be in the same subnet and represent another 32 addresses. The partitioning into sub-nets ensures that any potential broadcast storms are contained (The default behavior for Layer 2 is to broadcast if a destination address is not recognised whereas Layer 3 discards).
For portions of SPS network that are Layer 2, there should ideally be no active loops in its topology otherwise undesirable broadcast radiation that can result in a broadcast storm will occur. To ensure this is the case, IEEE 802.1Q-2014 protocol for rapid spanning tree is to be enabled. One minor implication is the reconfiguration time associated with the protocol. Any changes in the topology, such as equipment joining or leaving due to power up and down, with stop all traffic until the protocol has resolved which is typically the order of 100ms to 1 second. For this reason, it is common practice to keep as much of the network at Layer 3 as possible which is the main motivation for the SPS cabinet data switches being multi-layer.
The control and monitoring of the components of the network is implemented by MCCS in conjunction with TANGO. For commercial switches, SNMPv2 and SNMPv3 and Remote Network Monitoring Management Information Base, RMON, (IETF RFC 2819) and Remote Network Monitoring Management Information Base version 2 using SMIv2, RMON2, (IETF RFC4502) provide detailed status information that will interface to the TANGO framework. Where available, the option of monitoring individual flows within the network switches (as opposed to just packet counts on ports) is monitored.
Across SPS cabinets the network components are largely the same though may have minor differences in terms of transceiver type and supported number of links. These provide several communication capabilities, running at different speeds that support all the cabinet functions. This includes the connections communicating beam products to CSP as well as forwarding antenna data to the MCCS for calibration. Due to the number of potential links (from 256 SPS cabinets), to MCCS, the Control and monitoring data is communicated on the same physical 100 G bit/s link to the MCCS system. CSP destined data is largely communicated on 40 G bit/s Ethernet. The one exception being the CSP links

from the RPFs. In this case, 100 G bit/s is utilised to keep the number of fibres within the constraints of a single fibre ribbon between each RPF and CPF. Switches within the CPF convert these 100 G bit/s link to 40 G bit/s prior to forwarding the data to the CSP Correlator Beamformer, CBF. The 100 G bit/s links carry 6 station beams of data per link which is converted to 2 stations per link at the FFAA to CSP interface i.e. three 40 G bit/s links for every 100 G bit/s.

As illustrated in Figure 5-23, the SPS network within an SPS cabinet supports several link rates. The data delivered from TPMs is on 40G Ethernet links. Either 100G Ethernet or 40 G Ethernet, depending on location, is used for connections to or from the cabinet to CSP and MCCS as well as inter-data-switch connectivity. The QSFP modules appropriate to the link rate are populated in the switch.

Monitoring and Control data is passed at a lower link speed data through a 1G bit/s data network inside the rack including the Rack and Sub-rack management cards. This is connected to one of the main data switches through a 10 G bit/s link for onward communication with the MCCS and the Telescope Manager applications.

As there is no MCCS equipment in the RPFs, the SPS is used to relay control and monitoring messages between the MCCS and Field Nodes. This is purely connectivity within the SPS network and there is no SPS processing of these messages. The Control and Monitoring connections to each Field Node is via 1 G bit/s with one link for each APIU resulting in four links per station. To achieve this, two links (4 fibres) are interfaced via each Sub-rack management card.

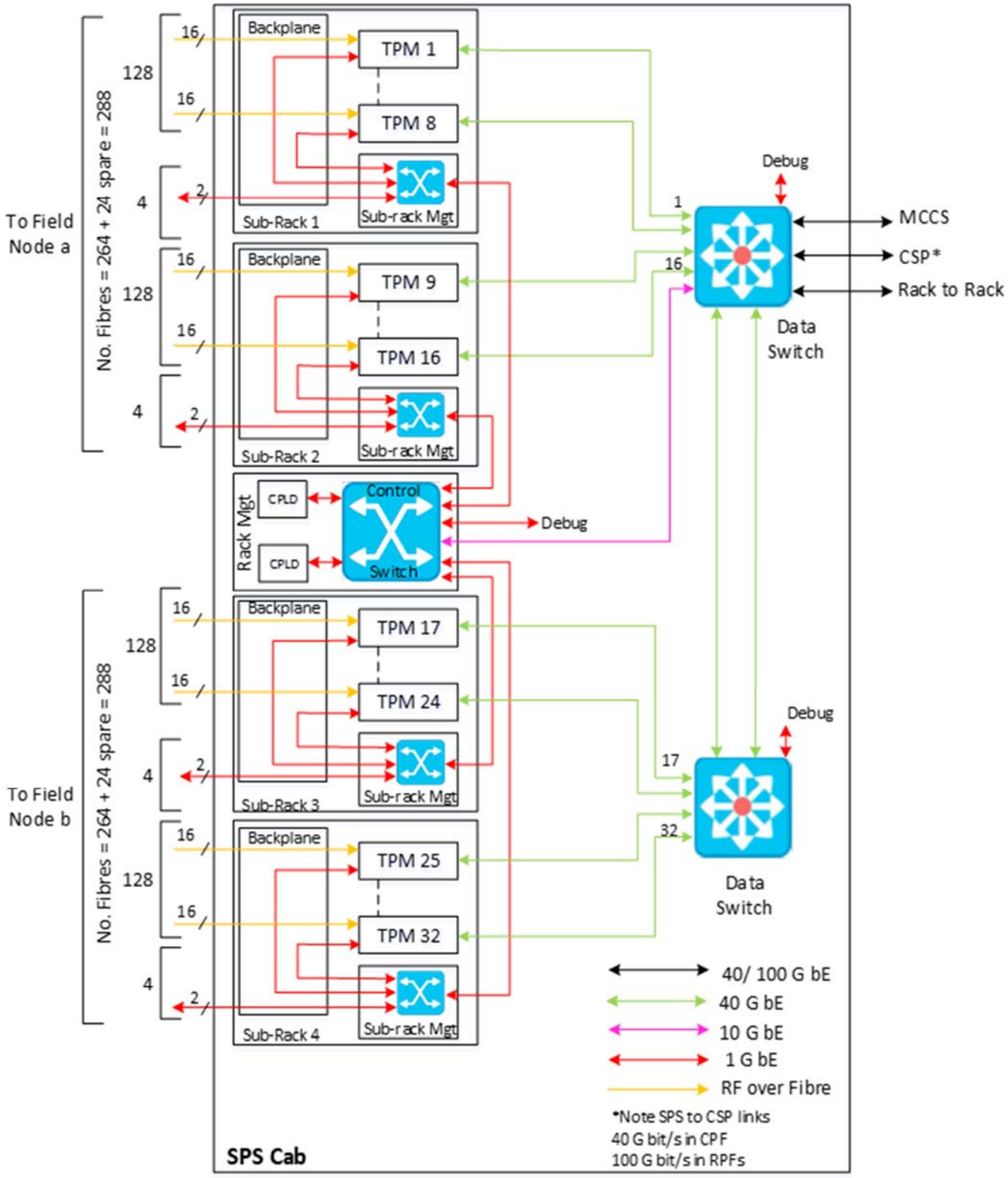


Figure 5-23 SPS cabinet level network

Currently, the 100 G bit/s switch market has converged on 32 ports in a 19-inch 1 rack Unit form factor with an example shown in Figure 5-24. In addition, a separate 1 G bit/s management is provided but in-band management can be implemented too. Provided an IP address is allocated to the switch management, the switch can be monitored or configured from anywhere on the SPS or MCCS network



Figure 5-24 32 port 100 Gb Ethernet Switch

5.4.3.1 *Security*

Although the principal security of the Low Telescope is not the responsibility of the LFAA, the LFAA network configuration provides reasonable steps to ensure the integrity of the SPS and LFAA whilst not restricting the functionality of the Telescope to the user. The aim is to provide protection from unauthorised users enumerating and gaining control of the network which might compromise the subsystem. This is particularly important for the network components as it is often difficult to detect whether they have been compromised. The following provides a representative list of measures easily taken across the main Data switches to achieve this integrity:

- The operating system will be periodically updated to the latest stable version considering the latest security advisories from the vendor.
- Access to the consoles is via login and strong passwords that are encrypted.
- All Aux or VTY access is disabled or accessed via login and encrypted strong passwords
- Access to network components is on a per user basis including separate accounts for each administrator such that there is traceability and accountability.
- TFTP is disabled for automatic configuration at reboot
- Reverse Telnet is disabled on all ports and SSH used in preference.
- Unnecessary protocols and services are disabled including:
    - ICMP redirects
    - ICMP broadcasts
    - ICMP mask replies
    - ICMP unreachable
    - Proxy ARP
    - Finger
    - BOOTP
    - HTTP access
- SNMP access to specific Hosts is restricted via the use of Access Control Lists
- SNMP v1 and v2 are disabled with a preference to SNMP v3
- SNMP v3 access is via authentication and encryption
- All SNMP management servers are secured
- Routing hash protocols for authentication are secured using MD5 and are not plain text

- Routing filters are applied at the LFAA borders are applied to prevent erroneous routing information from being injected to the network
- All routers use NTP to synchronise time
- NTP authentication is utilised to ensure only approved servers are used for synchronisation
- Logging time stamps are to include milli second granularity
- Logging is made available to the TANGO framework
- Access Control Lists are configured to log all access violations

5.4.3.2 *SPS Long haul links*

Figure 5-25 shows the layout of the spiral arms (North, South and East) of the LFAA within the boundary of the Boolardy station with the positions of the clusters of stations, including the Remote Processing Facilities. From this the length of optical fibre from each of the 36 RPFs has been extracted. The results are presented in Table 5-1.

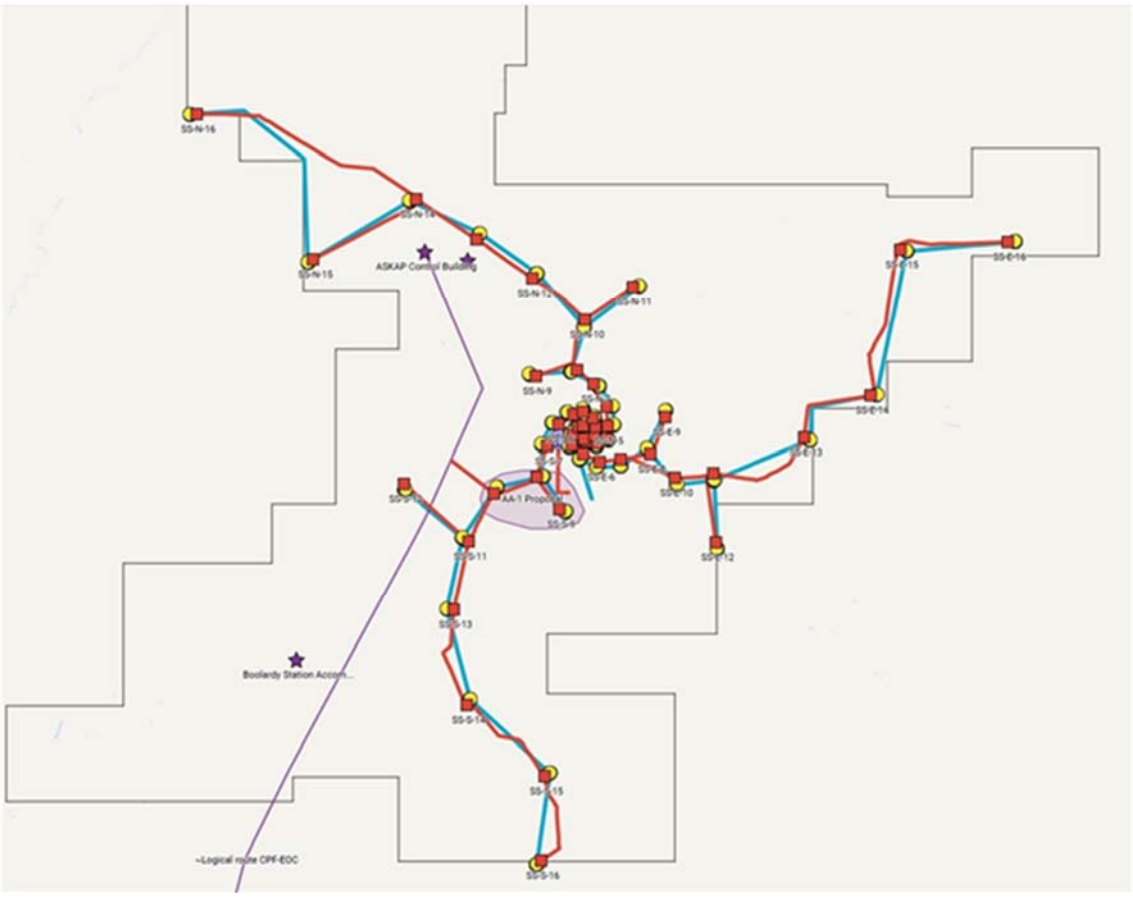


Figure 5-25 Spiral Arms of the SKA1 Telescope

Optical fibre length (km) from RPF to CPF for each spiral arm		
East Spiral Arm	**North Spiral Arm**	**South Spiral Arm**
1.6	5.5	1.8
3.0	7.0	3.7
4.9	8.8	4.3
7.4	11.3	5.2
10.6	14.6	7.6
11.0	15.0	8.0
13.9	20.3	12.8
19.3	20.6	18.1
22.1	26.1	18.7
30.2	32.2	25.5
41.7	41.5	33.9
50.2	60	41.1

Table 5-1 RPF Optical cable length to the CPF in km

Originally, SaDT provided a DDBH solution for communications between the SPS equipment in each of the remote stations and the central processing facility. This took the six SPS 100 G bit/s links (12 fibres) provided by the three SPS cabinets in each RPF and DWDM multiplexed them onto two individual fibres. These were then included as part of a twelve-way fibre ribbon shared with seven fibres used by SaDT. However, an ECP (1700010) was raised by the cost control project that removed the DDBH on the basis that the implementation of point to point links would be cheaper.

For RPF to CPF distances up to 25km fibre length point to point links can be implemented using QSFP-28 LR-4 or ER-4 transceivers fitted to the SPS data switches. In this case, each RPF connects via four fibres supporting support two 100 G bit/s (one for CSP and one for MCCS destined data) within the same optical fibre ribbon as the 7 already used by SaDT. The shaded areas of Table 5-1 indicate the twenty-six RPFs that will utilise this connectivity. Of these, the inner thirteen RPFs will have transceivers of type LR-4 whereas the outer thirteen utilise transceivers of type ER-4.

The ten RPFs with fibre lengths greater than 25km (but less than 60 km) utilise a DDBH like solution with coherent optics to achieve the transmission length. This solution utilises Muxponder equipment with the total capability of up to 200 G bit/s on the DWDM inter facility links. Consequently, only two fibres are needed for each of the outer RPF to CPF links.

Muxponders are available from several manufacturers will typically take up 3U of rack space at either end of the link. For the CPF this is 30U of rack space with a total of 10 muxponders supporting the 10 outer RPFs. These will be in the cabinets in the CPF reserved for DDBH. Each Muxponder dissipates ~ 350 Watts i.e. an extra 350 Watts in each RPF and 10.5 kW in the CPF.

5.4.3.3 *SPS Station Level Network*

The station level network provides the capabilities summarised in the diagram and in the table below. For each communication data the expected bit rate, the used network, the calculated channel occupancy, the packets per second, the required number of connections and the required number of the cable interface are listed.

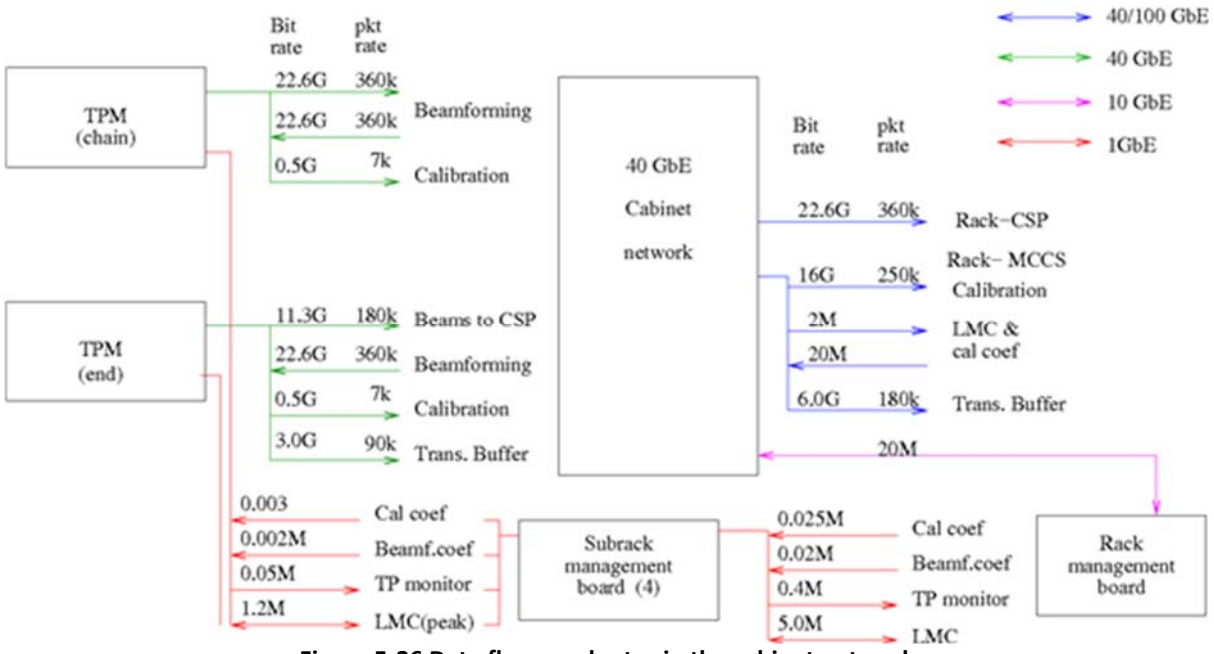


Figure 5-26 Data flows and rates in the cabinet network

Beamforming	Bit rate	Network	Occupancy	Pkt/sec	n° conn	Cable
TPM ->TPM beamforming 16 bit IN, 8 KB	22.6 G	40G	56,5%	360 k	15	16 QSFP
TPM ->TPM beamforming 16 bit OUT	22.6 G	40G	56,5%	360 k	15	
TPM-> 40G SW beamforming 8-bit OUT	11.3 G	40G	28,3%	180 k	1	
Transient buffer MCCS						
TPM -> MCCS calib spigots, 8 kB	0.5 G	40G	7.5 %	90k	1	
Calibration Spigots						
TPM -> MCCS, calib spigots, 8KB	0.5 G	40G	1,3%	8k	16	
Sub-rack management						
MCCS -> sub rack management	5 M	1G	0,1%	2000	2	2 RJ45
sub rack management -> MCCS	3 M	1G	0,3%	2000	2	
subrack man -> TPM, raw coeff	2 k	1G	0,0%	1	16	
sub rack management <-> TPM	1.2 M	1G	0,1%	500	16	

Table 5-2 Station Level Network

For each station a 40G Ethernet data network and a 1G Ethernet management network are defined, joined together at cabinet level.
In the beam-forming the TPMs inside each station are connected with a cabinet 40G data network to share the partial beam data with 16-bit resolution at 22 Gbit/s of data rate.
The TPMs are connected logically in a serial chain: the first TPM generates the first internal beam-form data to the second one that adds the contribute coming from the corresponding antennas and propagates it. The last station TPM generates a half resolution beam-form data that is transmitted as station output.
Each TPM provides one 40G Ethernet port on a QSFP interface, while the second one QSFP available on the board shall be left unconnected or removed if no upgrade capabilities will be requested (TBC).

Each TPM also continuously generates calibration data that are received by the MCCS computer in the LFAA network, outside the cabinet. The MCCS computer sends back raw calibration data to the Sub-rack management board that elaborates and distributes to each TPM on the same network.
Each station generates also a Transient Buffer data that are either delivered continuously to the MCCS on the 40G Ethernet network, or stored locally in TPM DDR memory and uploaded to the SDP on request. In this latter case the upload will involve at most 2-4 TPM at any given time, in turn.
The beam-forming, the calibration and the transient buffer data are shared with 8KB UDP packets, without flow control and retransmission capabilities.
It is also requested that communication packet ordering transmitted with the UDP is respected to allow raw data reconstruction. Corrupted or out-of-order packets in the beam-forming data will be discharged. The maximum bit and packet error rate shall be defined to guarantee that the total number of corrupted or missed packets to CSP will not exceed a TBD fraction, in order not to degrade the final SNR. Corrupted packet in the calibration data and management data shall be recovered by TCP protocol that manages consistency check and retransmission.
The management 1G Ethernet network connects the 8 sub-rack TPMs to the sub-rack management board with direct UDP access through the backplane and the local switch (integrated in the management board itself). The sub-rack management board then can communicate through TCP or UDP with the cabinet level management network by means of one or two copper gigabit cables with RJ45 interface.

5.4.3.4 *Cabinet level network*

The cabinet level network connects the internal stations and provides the connection to the CSP, the MCCS and the surrounding cabinets.
The proposed implementation is detailed in the figure below.

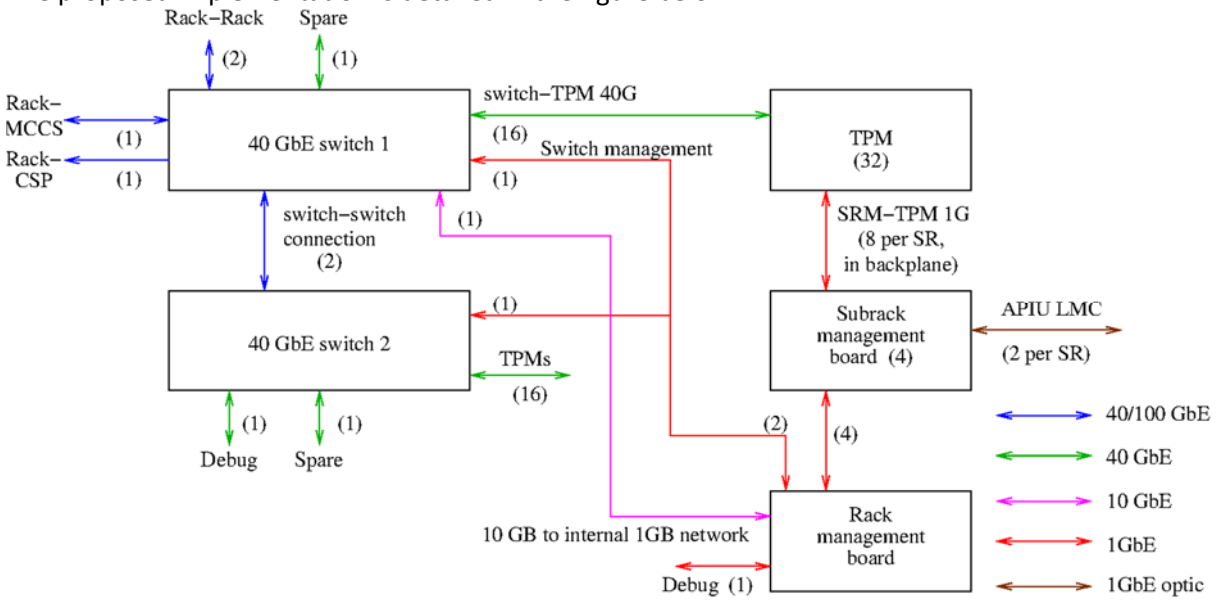


Figure 5-27 Cabinet Level Network

If a 100G uplink can be available to the CSP, the cabinets are locally joined together to reduce the number of connections from the LFAA data network to the CSP data network.
The 1G cabinet management network is connected to the 40/100G LFAA data network by the external side and to the STATION management network to the internal side. Also, on this network the other cabinet elements are connected: power distributor, heat exchanger and so on. Cabinet level network is conditioned by the commercial network switches available from the market. Two switches are needed to implement the 40/100G cabinet network and the connection between the switches should

be considered. The upper switch hosts all external connections. In this way a switch failure of the lower switch would cause a loss of only one station.
Connections required at cabinet level are listed in the table below, together with related characteristics and aggregated traffic.

Management 1G Network	TX	Occupancy	RX	Occupancy	Network	Pkt/sec	n° conn	# QSFP Ports
40G Uplink	3,00E+06	0,0%	7,00E+06	0,0%	40G	1,09E+02	1	1
Rack management board	1,00E+06	0,0%	1,00E+06	0,0%	1G	1,56E+01	1	
Station 0 management	1,00E+06	0,0%	3,00E+06	0,0%	1G	4,69E+01	2	
Station 1 management	1,00E+06	0,0%	3,00E+06	0,0%	1G	4,69E+01	2	
Management spare					1G		0	
Cabinet maintenance					1G		1	
Stations data 40G Network	TX	Occupancy	RX	Occupancy	Network	Pkt/sec		
Station 0 beamforming 16 bit, TPM <-> TPM	3,39E+11	56,5%	3,39E+11	56,5%	40G	1,08E+07	15	16
Station 0 beamforming, 8-bit, TPM -> 40G	1,13E+10	28,3%			40G	1,80E+05	1	
Station 0 calibration, TPM <-> TPM	8,00E+09	1,3%	1,60E+06	0,0%	40G		15	
Station 1 beamforming 16 bit, TPM <-> TPM	3,39E+11	56,5%	3,39E+11	56,5%	40G	1,08E+07	15	16
Station 1 beamforming, 8-bit, TPM -> 40G	1,13E+10	28,3%			40G	1,80E+05	1	
Station 1 calibration	8,00E+09	1,3%	1,60E+06	0,0%	40G			
Switch <-> Switch	TBD		TBD		40G	TBD	2	2
Station 0 spare						0	0	1
Station 1 spare							0	1
External Interfaces	TX	Occupancy	RX	Occupancy	Network	Pkt/sec		
Rack, (2 Station) -> CSP, beamforming	2,26E+10	56,5%	0	0,0%	40G	3,60E+05	1	1
Station -> CSP spare					40G	0,00E+00	0	1
Rack, (2 Station) -> MCCS, spigots	1,60E+10	40,0%	0	0,0%	40G	2,55E+05	1	1
MCCS -> Rack (2 stations)	0,00E+00		3,20E+06	0,0%	40G	5,10E+01	1	0
MCCS -> Rack, Spare					40G	0,00E+00	0	1
Rack <-> Rack , Option, IN	2,26E+10	56,5%			40G	3,60E+05	1	1
Rack <-> Rack , Option, OUT			2,26E+10	56,5%	40G	3,60E+05	1	1
Rack <-> Rack , Spare					40G	0	0	1

Table 5-3 TPM Cabinet Network

The network is managed as a single sub-net as described in section 5.4.3.4.

The connection to the CSP can transmit the station beam-forming data outputs on a single aggregated connection. Direct connection to the CSP is expected.
Similarly, the station connection to the MCCS aggregates the calibration data and the management data. A connection to the MCCS internal network is present every two cabinets (CPF) or every three cabinets (in RPF). The rack-rack connection ring allows for some redundancy in the MCCS control link, at least in the CPF.
Switch level spare ports are to be provided, to allow at least one free port for each switch.
As mentioned in the station network level, the maximum bit error rate, the number of packets for second allowed, the packet ordering shall be considered in the final design.
Let us consider the packet ordering of the station output beam-forming: if the generated packets are equally distributed, the expected packet-to-packet latency is about 5.8 us (1.6 us is the time requested for an 8 Kbyte packet on the 40G network and 4.22 us is the expected time between successive packets). If the involved switches can assure a maximum propagation latency below that, it can be assumed that the transmission ordering will be preserved on the network.

5.4.4 SPS Rack Assemblies

Cabinet elements are summarised in the following table, Table 5-4.

Description	n°	Rack Unit	Positioning
Processing			
TPM sub-rack	4	6	19" column
40G Eth switch	2	1	19" column
Rack Management	1	1	19" column
Cooling			
AIR to liquid exchanger	1	0	Side
Liquid to liquid exchanger	1	0	19" column
Pumps	4	0	Below
Expansion vessel	1	0	Below
Powering			
General power, manual	1	1	Side/19" column
Power distributions, actives	-	-	Side/19" column
Mechanics			
External chassis	-	-	-
Internal supports	-	-	-
Cabling elements	-	-	-

Table 5-4 TPM-sub-rack-based cabinet elements

Current proposed design is compatible with a standard chassis available on the market (e.g., ABB customised by RGM mechanical company).
The cabinet is not shielded at chassis level, if all the internal elements are properly certified for EMC. This policy confirms the one followed by AAVS1, where the TPM board has been certified with good results by the Australian laboratory. The preliminary schematic layout is shown in Figure 5-28.

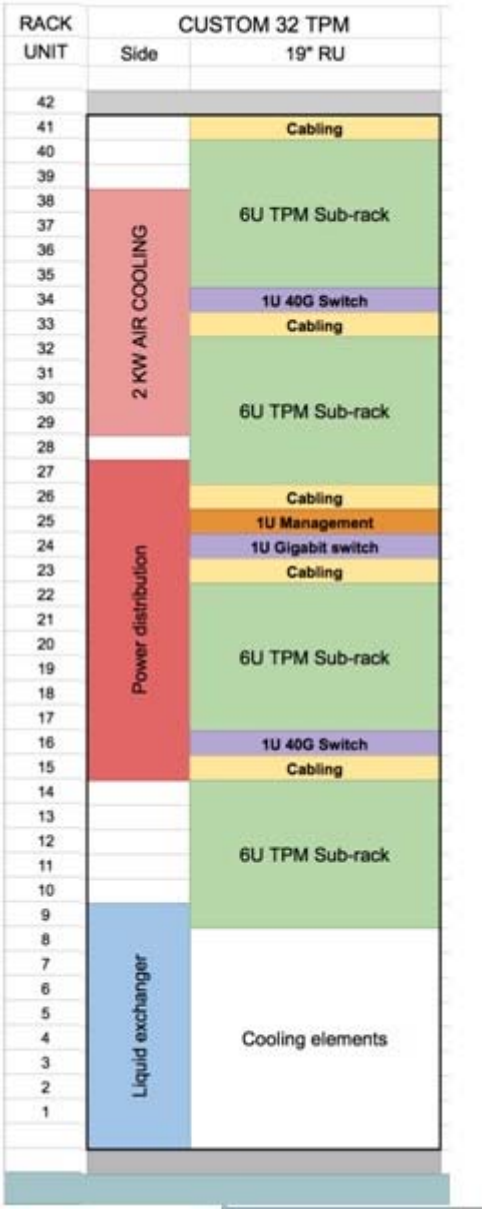


Figure 5-28 Cabinet preliminary layout front view

The Power distributor element implements the general on/off switch, with manual activation and the required safety passive protections.

The power distribution unit manages all the controlled switches that can power all the other cabinet elements, with exception of the management board that shall be always powered.

The TPM sub-rack will be possibly coupled with the 40G Ethernet switch placed in the middle to implement a complete station module. With this approach the 40G QSFP connection are short and local and all the TPM of a single station are connected to the same switch to assure communication efficiency.

In Figure 5-28 the yellow cabling units are empty space for fibres and general cabling to allow maintenance capability and the possibility to extract a single TPM without other cable removal.

The cabinet management and the 1Gbit management switch (optionally considered but not in the baseline design) can be placed in the middle or everywhere in the 19" column. The middle position can be optimal for clock cabling and network connections to each sub-rack.

The liquid cooling circuit is placed on the bottom, with the liquid exchanger connected with the infrastructure liquid circuit by one side and to the cabinet internal circuit on the other. Also pumps

and other liquid elements shall be placed on the bottom of the rack, with exception of the expansion vessel that shall be placed above the liquid circuit, to allow air removal and maintain the selected secondary pressure. A detailed description of the cooling sub-system can be found in[RD12].
The cabinet mechanics respects all the infrastructure specifications [AD35] in terms of occupied volume, maximum weight, available maintenance space, air and liquid floor interface, optical fibre interface from the top.
A possible cabinet complete design is presented. All the cabinet elements have been integrated with standard elements, where available, considering installation and maintenance processes.

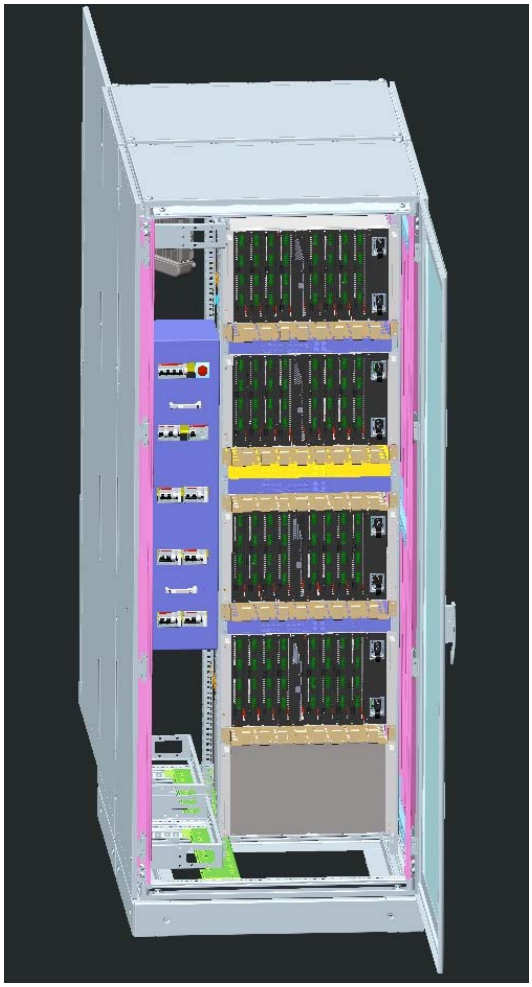


Figure 5-29 SKA LFAA TPM cabinet main elements

In the proposed design, two, standard, 80 x 60 cm^2 rack structure have been paired to obtain the requested 80x120 cm2 external volume of the cabinet. This solution allows standard catalogue component selection and a robust structure, with IP55 feature, see Figure 5-29 and Figure 5-30.
Cabinet internal layout has been organised with two internal main volumes, the 19” rack column on the right and a 20 cm side on the left.
On the cabinet front side, a single port has been selected, opening on the right, with a transparent glass to allow the vision of the status lights of the present elements by an operator.

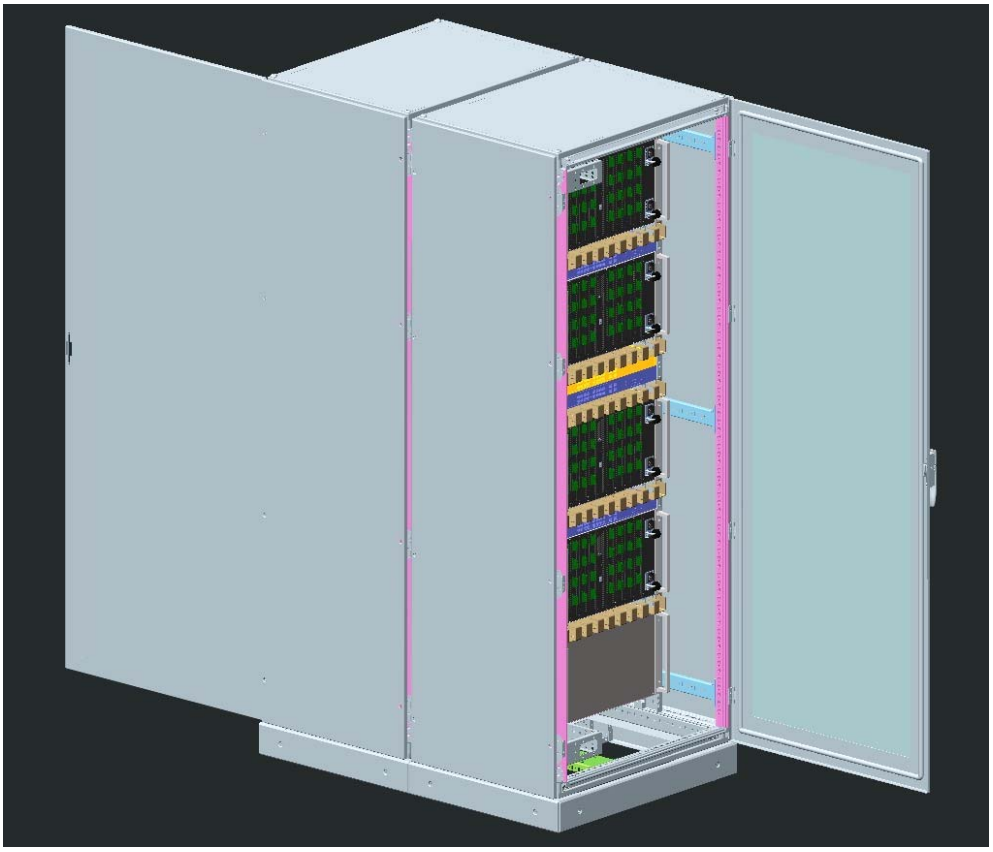


Figure 5-30 Cabinet double doors with glass on the front side

On the cabinet back side, a metal door has been chosen to allow practical maintenance access to the cooling circuit and to the connection elements from the infrastructure.
A standard footer, a top and side metal enclosures will complete the external body of the cabinet, ensuring the requested inner volume separation from the building.
The Infrastructure specification document guarantees 90 cm of free space in front and on the back side of each cabinet, allowing the complete opening of the doors providing a simple access to the internal elements.
The 19” rack column will house the TPM sub-racks. This column has more than 20 cm of space in the front before the door to allow practical cabling for the front panels and a small space, about 4 cm on the left, for fibre and power routing from the top to the TPM front panel.
The internal structure is built with a combination of standard elements and custom parts.



Figure 5-31 SKA LFAA cabinet layout, main concept & metallic structure

The 19” rack elements are standard elements but for the insertion of the sub-rack custom guides have been designed (orange in the picture of Figure 5-31), integrated with the cabling unit to provide the required support for sub-rack insertion and extraction. (L3-131). Each individual element can be removed without the need of removing other unrelated elements. All required electric and cooling connections can be disconnected using the front and rear door accesses (L3-129).

The metallic guides for the sub-rack are placed in the volume of the 1U cabling space, to maintain the standard vertical step.

Each sub-rack and the cabinet management board have below a cabling unit to allow the routing of the required cables with minimal usage of the elements front panel, mainly to simplify the cabling and the element removal. Each connection type uses physically different connectors, to preclude the possibility of equipment damage by incorrect connection (L3-130).

On the bottom of the 19” rack column, a closed volume will house cooling liquid circuit elements (shown open and empty in the Figure 5-31), to minimise interaction with the electronics circuits and to interface with the infrastructure incoming cooling liquid interface from the floor.
The small size elements of the cooling circuit will be pre-assembled in this element with the interface valves accessible from the rear side of the column (Figure 5-32 and Figure 5-33).

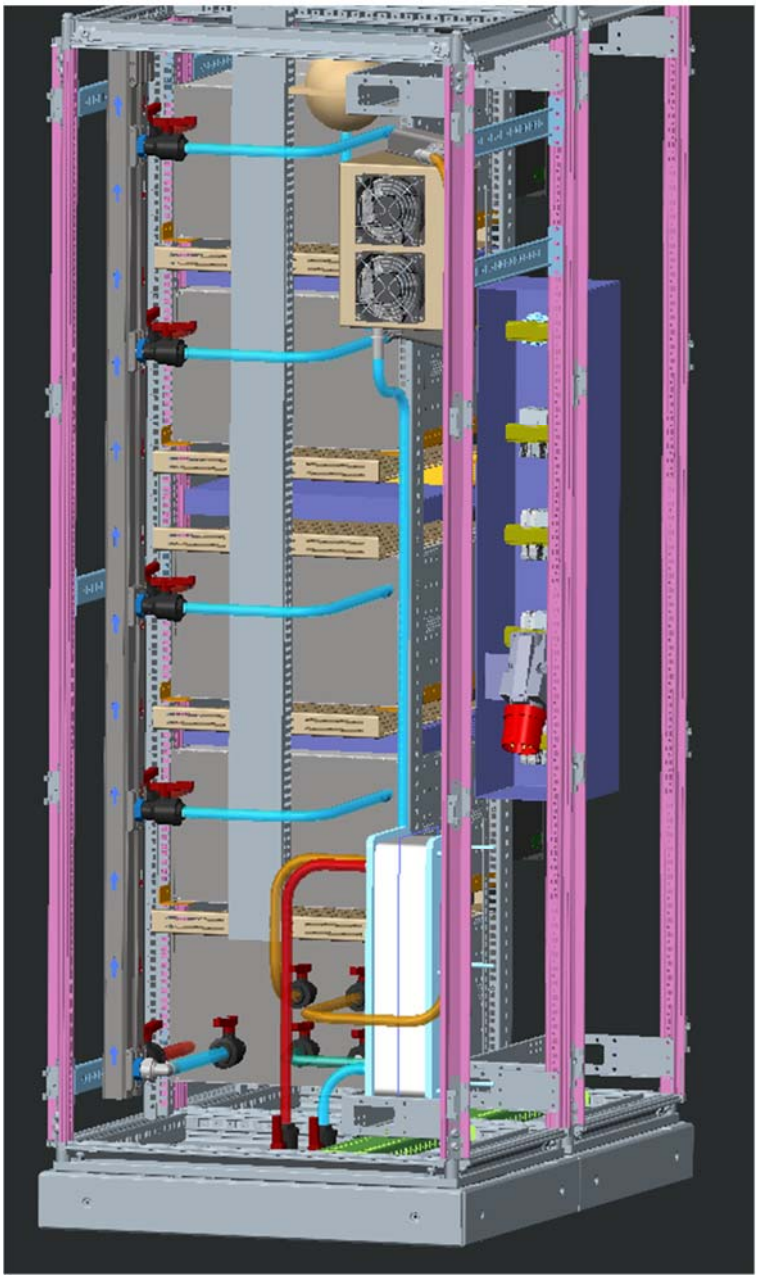


Figure 5-32 Cabinet back access, backdoor hidden, cooling circuit and power input

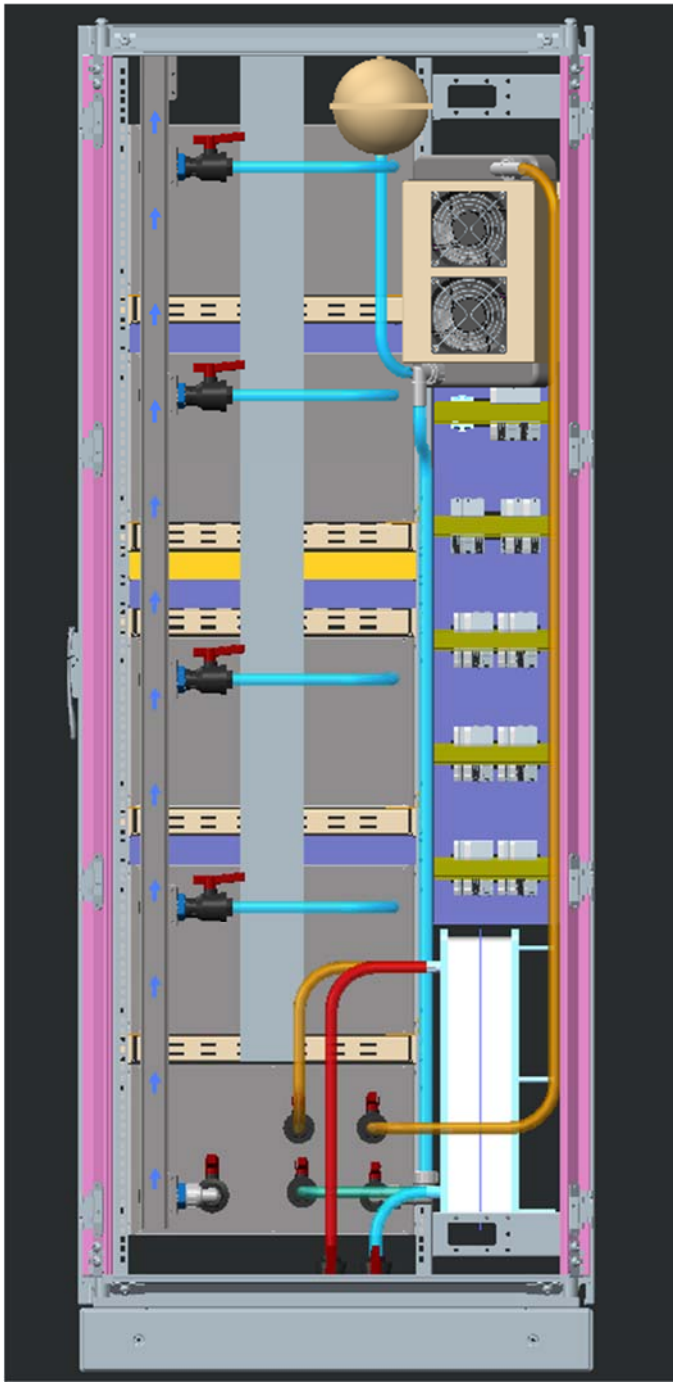


Figure 5-33 Cabinet back side

With current 19” rack elements, the maximum depth is below 50 cm, resulting large free space behind the column element to the back of the cabinet. In this volume all the remaining elements of the cooling circuit will be placed: the pipes, the liquid to liquid heat exchanger, the manifold, the liquid to air heat exchanger and the expansion vessel.

The infrastructure cooling pipes that come from the floor are connected, by two valves, to the liquid to liquid heat exchanger placed on the right, close to the floor (within the pictures). The pipe of the internal circuit coming from the exchanger are connected to the volume containing the pumps and the other small cooling elements from which they come back to the manifold (on the right) and to liquid to air heat exchanger on the left.

The manifold is a vertical, metallic structure that takes the output from the pumps placed on the bottom and distributes almost uniformly the liquid to the several drains present in the circuit, the sub-rack liquid cold plates and the liquid to air exchanger. The same element collects the heated liquid back to the bottom to close the circuit (light blue pipes for the cold liquid, red pipe for the hot liquid in the pictures).
Each unit collected to the manifold can be separated by a valve for maintenance removal with a small liquid dispersion. The pipe and valve distribution routing will exclude the natural contact between liquid and electric power distributing elements.
With this approach the liquid-to-air exchanger is placed on the backside of the cabinet, on the top-right above the electric power distribution reserved volume.
Two fans that force the air through the radiator element complete the air to liquid radiator. The related air direction shall be chosen conforming to the choice done for the fans present in TPM the sub rack elements. The internal position of all the cabinet elements shall be optimised to allow the flow of the internal air between the front side and the rear side.
The expansion vessel is placed over the liquid to air heat exchanger in the upper part of the cabinet to collect possible air present in the circuit and stabilise the pressure due to possible temperature variations.
Some valves required for the filter insertion and the filling of the circuit are not shown in the current drawings.
Thanks to the low pressure and low temperature of the circuit, high quality silicon flexible pipes have been proposed for all the internal circuit connections, simplifying the construction and the maintenance.
The electrical components, related to the power distribution and the required protections are inserted in the left space of the cabinet, inside a metallic box.
All the main function and protection circuits are directly accessible from the cabinet front panel and the connection to the rack element can be done with directly cabling from the rear or from the side.
The metallic box will provide a standard DIN guide to allow the usage of standard elements to implement the electrical circuit described in the previous section.
Some status lights and emergency buttons will be placed here for quick access to the maintenance operators.

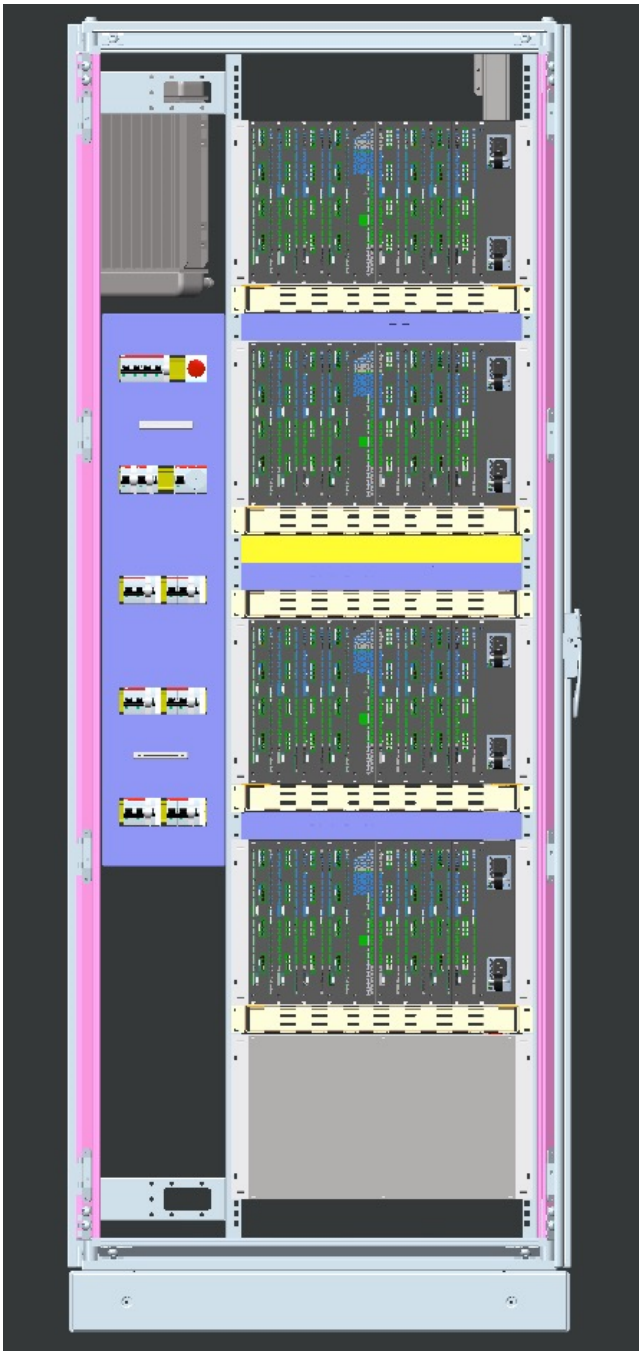


Figure 5-34 Cabinet layout front view

Further details concerning the Cabinet can be found in [RD12]

5.5 Firmware Components

In this chapter the main TPM functional blocks are described. The TPM is organised in two main sections: the management and control plane and the acquisition and processing plane. The management plane is built around a FLASH based Lattice MachXO2 CPLD, and includes a 1Gbe Ethernet connection, EEPROM and SPI FLASH memories, and the interface to the Analogue Front End (preADU).

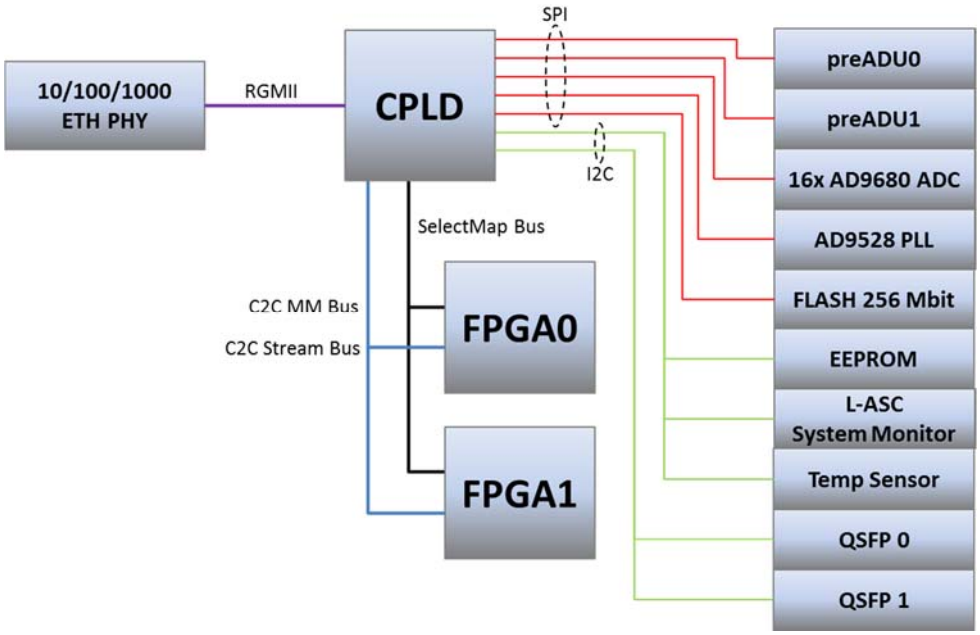


Figure 5-35 Control plane of the TPM firmware

CPLD firmware is stored on the internal CPLD FLASH memory. It is auto-configuring at board power-up and manages the access to the device registers through the 1GbE control interface, using the UDP based Uniboard Control Protocol. It also provides a master UDP streaming capability, sending over the 1GbE the packets received on the Chip-to-chip (C2C) streaming bus.
FPGA firmware is identical on the two devices. It is composed of two layers: An input-output ring, with physical interfaces (mostly based on vendor specific IPs) encapsulated in a device agnostic wrapper, plus specific generic functionalities (e.g. PPS and clock management, UDP Ethernet layer). The actual signal processing is performed inside a DSP layer, which receives packetised and synchronised samples, and generates packetised processed samples.
Currently, developed firmware code partly follows “Fundamental SKA Software and Hardware Description Language Standards” [RD2]. Good practice and style guides are followed in coding. All main firmware modules are documented in detail, using UML syntax (e.g. [RD79] [RD80]). Code is self-documenting and maintained using a version control system. Most modules have a regression test to allow automatic verification of module performance. Code update is automated using simple procedures.
At present, [RD2] is not fully enforced and as such will require further work as part of Bridging.

5.5.1 FPGA IP Blocks

FPGA firmware structure is described in detail in [RD14] and shown in Figure 5-36. It is composed of a ring of physical interfaces and general functionalities, surrounding a DSP layer performing the actual signal processing. Modules in this I/O ring are described in section 5.5.1.1 The DSP layer structure is shown in Figure 5-37 and DSP modules are described in section 5.5.1.2. Each block uses standard interfaces for streaming packetised input and output samples, and for control (not shown in the diagram). Stream clock domain is colour coded in the diagrams. Main clock domains are the ADC clock (not oversampled) and the DSP clock (oversampled). Other clock domains are related to the specific hardware interfaces.

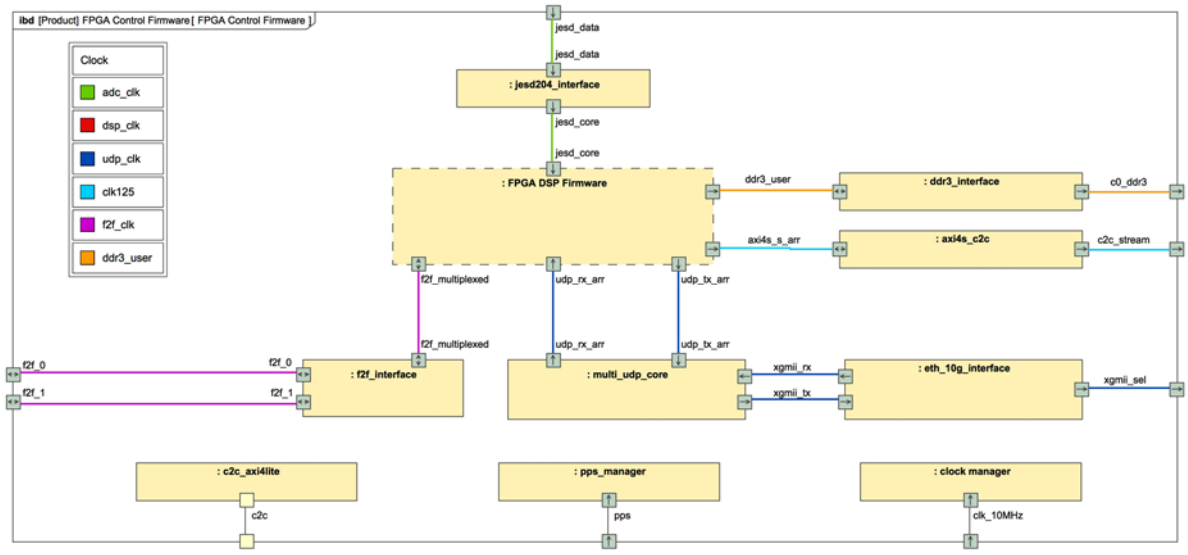


Figure 5-36 Input/output ring of the FPGA Firmware

Main firmware blocks are listed in Table 5-5. When ownership is not listed, module has been developed in the LFAA design consortium.

PBS ID	Name	IP owner
	CPLD Firmware	Sanitas SG
	JESD204_interface	
	JESD204_IP	Xilinx
	DDR3_interface	
	DDR3_IP	Xilinx
	Multi_UDP_core	RAL
	Clock_manager	
	PPS_manager	
	C2C_axilite	
	F2F_interface	
	F2f_phy	Xilinx
	Axi4s_c2c	
	Test_generator	
	Total_power_RFI	
	channeliser	
	Tile_beamformer	
	Station_beamformer	
	LMC_Calibration_sample_generator	
	LMC_spectrometer	

Table 5-5 SPS IP Blocks

5.5.1.1 *SPS I/O Ring IP modules*

The Input/output ring modules include both internally developed modules and third-party IP cores.

Developed Firmware modules are:

- ***AXI4Lite Infrastructure***. It consists of a set of configurable modules for implementing memory mapped register interfaces. The infrastructure includes AXI4Lite Bus Slaves and the logic to connect multiple slaves in a shared bus configuration. The VHDL code is automatically generated by a Python script which can process an XML description of the required memory map.
- ***C2C to AXI4Lite interface***. An AXI4Lite master interface, controlled by the CPLD using the C2C Memory Mapped Protocol. Allows MCCS to access, control and monitor the FPGA modules on the AXI4Lite infrastructure using the 1 Gb Ethernet interface.
- ***AXI4Stream Infrastructure***. It consists of a set of configurable modules implementing the AXI4Stream protocol interface. The set includes packer, un-packer, mux, de-mux, FIFO, packet buffer, adder, rounder, packet arbiter, pipeline module, etc. Each module is re-usable in different contexts by means of VHDL generics.
- ***AXI4S C2C Bridge*** The main purpose of this module is enabling the FPGAs to communicate to the CPLD using a channel having a throughput close to 1 Gbit/s. This interface is used to transmit streaming UDP packets from the FPGA to a fixed destination, over the Gigabit link managed by the CPLD.
- ***FPGA2FPGA (F2F) Link***. The F2F module is based upon the Xilinx Select-IO IP core, which manages 18 LVDS lanes each running at 1.25 Gbit/s. Two Select-IO IP cores are used to manage the two sub-links that compose the F2F link. Each F2F sub-link can be configured either as input or output link at configuration time. When the F2F sub-link is configured as output link in one FPGA, the corresponding F2F sub-link in the other FPGA must be configured as input link to avoid conflicts on the F2F bus. In this way the F2F link can be configured as a bidirectional link supporting 22.5 Gbit/s in each directions or mono-directional link supporting 45 Gbit/s in only one direction. A separate module handles the different clock domains, mapping the physical 18 LVDS lines to two unidirectional parallel streams, running in opposite directions, each with 105 lines at 200 MS/.
- ***40G UDP Core*** The 40G UDP core receives/transmits UDP packet from/to the network. When transmitting an UDP packet it manages the packetization of the user data taking care of UDP, IP and Ethernet headers. In the same way, received frames are parsed and related frames are decoded to provide the UDP payload to the user logic.
- ***DDR3 Interface.*** This is a wrapper around the Xilinx Memory Interface IP core. The user interface consists of separate address and data busses and few control signals permitting to have seamless access to the external DDR3 devices.
- ***PPS Manager.*** The PPS manager contains the logic used to sample the external PPS signal and generate an internal PPS signal that is synchronised across multiple TPMs to the single ADC sample
- ***Clock Manager*** The clock manager generates al the required clock frequencies inside the FPGA.

The following externally developed IP cores have been used inside the design

- ***System monitor.*** The System Monitor module is a Hard IP core providing ADCs for digitizing external voltages, on-chip supply voltage sensors and FPGA temperature sensor. Digitised values are written into specific registers that are memory-mapped on the AXI4Lite bus.
- ***Axi4Lite DRP Bridge.*** The AXI4Lite to DRP Bridge provides access to the Dynamic Reconfiguration Port implemented in several Xilinx primitives. The Xilinx primitive connected

to the DRP Bridge are all GTH transceivers used in the JESD204B and 40G cores, related QPLLs. For each of these devices the corresponding DRP register are mapped transparently to the AXI4Lite bus at specific offset.

- ***Xilinx DDR3 Memory IP*** Xilinx provided DDR3 IP core version v1.2 (Rev. 1), used inside the DDR3 Interface
- ***JESD204 IP*** Xilinx provided JESD204B IP core version 7.0 (Rev. 1), used inside the JESD204 Interface
- ***SelectIO Interface*** Xilinx provided SelectIO Interface IP core version 5.1 (Rev. 7). It is used for managing fast LVDS lines in the F2F Interface.
- ***40G UDP Core*** RAL provided 40G UDP core. The 40G UDP core receives/transmits UDP packet from/to the network. When transmitting an UDP packet it manages the packetization of the user data taking care of UDP, IP and Ethernet headers. In the same way, received frames are parsed and related frames are decoded to provide the UDP payload to the user logic
- ***40G Ethernet PHY*** RAL provided 40G Ethernet PHY using Xilinx GTH transceivers.

5.5.1.2 *SPS DSP layer IP modules*

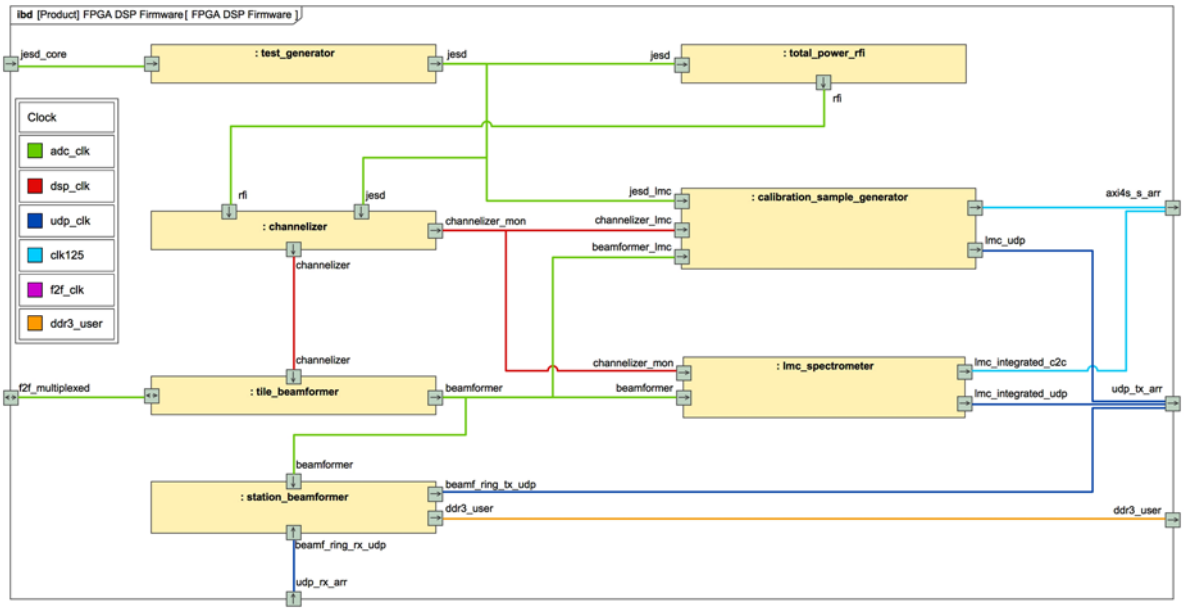


Figure 5-37 DSP layer of the FPGA Firmware

All the modules in the DSP layer have been internally developed.

- ***Sample test generator.*** The Sample Test Generator module can synthesise a test signal that is obtained by mixing the following components:
    - 2 signal tones with independently specified phase and frequency
    - Pseudorandom noise
    - Periodic pulse

  Tones are generated by a direct digital synthesiser, with a frequency resolution of 31 bits (0.37 Hz/step) and a phase resolution of 2048 steps/turn. The pseudorandom noise is obtained as the average of 8 uniformly distributed 8-bit signed values. The resulting distribution is almost Gaussian, with zero mean and a standard deviation of 26.179 ADC units. The kurtosis is 2.85, slightly flatter than for a true Gaussian. The periodic pulse is a single nonzero sample of nominal value of 127 ADC units, which is repeated from 1 to 16 times in each 864-sample frame. All signals can be synchronised to a specific time, to have the same signal across

multiple TPMs. Amplitudes of each signal component can be independently specified, as an 8-bit signed quantity in the range 0 to 255/256. The maximum values for the tones and the pseudorandom noise RMS level 31.875 and 26.03 ADC units, respectively. The generated test signal can substitute the data from all or a subset of the acquired antenna.

The module includes a static delay for each input signal by an integer number of ADC samples in the range of 0 to 255 ADC samples, allowing for compensation of cable delays. Nominal delay is set to 128 samples, to allow both positive and negative delays.

- ***Channeliser.*** This module implements the following functions:
    - Channelization. It performs a channelization in frequency of the input samples for all 16 signals (8 antennas, 2 polarizations), using a polyphase oversampled filter bank. Produces a set of 512 complex frequency channels for every 864 input real samples. The implemented Channeliser is composed of a polyphaser filter and a real valued input FFT engine.
    - Post-FFT equalization by application of power-of-2 divider parameters which are defined for each frequency channel from each antenna. Parameters can be programmed via AXI4Lite registers. Each parameter specifies the number of LSB to round off the 20+20 bits Channeliser output sample to obtain a 12+12 bits data sample that is forwarded to the next stage of the DSP chain.
    - Forwarding of channelised and equalised data to LMC modules including data width reduction and rounding to 8 bits

  Module has been optimised for the Xilinx Kintex architecture, using the multipliers at double clock rate. A vendor agnostic not optimised version of the IP is also available. Filter coefficients are specified in a VHDL file, generated by a Matlab procedure from filter specifications. Output frame is rotated to always have a sample that is a multiple of 1024 samples as the first sample in a frame. This prevents frequency rotation of the PFB channels. The FFT uses 18-bit arithmetic up to the final stage, which uses 20-bit accuracy. The channeliser never saturates up to input sample amplitudes of 70 ADU RMS at the ADC, which is outside the linear operation range for the ADC. In any case, samples that are truncated at any processing stage are flagged. Samples can also be flagged by the RFI wideband.
- ***Tile beamformer***. The Tile Beamformer performs the following functions:
    - Selection of up to 16 spectral regions. Regions may repeat and overlap. They represent different beams, subarrays, or simply disjoined parts of the spectrum. The total number of channels in all regions is limited to 384 (300 MHz).
    - Delay correction is performed for each beam, by applying a phase correction proportional to the delay and channel frequency. Delay is computed internally to the module using a linear approximation (start delay and delay rate). Delay centre is common for all antennas in a station.
    - Calibration of each channel, including correction for polarization errors and rotation. Calibration is specified as a complex 4x4 matrix for each antenna and channel.
    - Requantisation to 12 bits of the result. This allows for bit growth using 16 bits samples in the station beamformer travelling sum.
    - Tile beamforming. Aligned antenna signals are summed together. Odd and even channels are exchanged among FPGAs, with FPGA0 processing even channels and FPGA1 odd channels.

  As at most 384 channels are selected, after the first block the signal is processed using the 200 MHz ADC clock. At this stage a frame is composed of 192 (odd or even) complex, 12+12-bit samples. Correspondence of logical channels to physical channels depend on programmed values in the selection block.
- ***Station Beamformer.*** The Station Beamformer performs the following functions:

- 8 input frames of tile beamformed samples are stored in a FPGA internal memory buffer. These samples are then stored in DDR memory in time order, in blocks of 4 consecutive channels.
- In the first TPM serving a station, blocks of 256 consecutive samples, 2 polarizations, 4 frequency channels are framed in a UDP packet, together with a simplified SPEAD header, and sent to the 40G link via the UDP formatter
- Other TPMs wait for incoming packet, retrieve from DDR memory the corresponding packet, sum the two together and send the resulting packet to the 40G link
- Last TPM in a station reformats 8 packets into 4 separate packets for the CSP (one per channel, 2048 samples each). CSP samples are requantised to 8 bits
- Last TPM also reformats these packets for the transient buffer storage, on the MCCS servers.
- A SPEAD header with relevant information is prepended to all packets

Memory access uses the protocol defined by the DDR3 Interface module. Burst size and access arbitration ensures an efficient memory usage.

- ***Total power and RFI detection.*** The total power for each input signal is calculated in parallel on all antennas and polarizations. Total power level can be used to set the preADU attenuators to the optimal ADC input level, and in general to assist the calibration. The integrator keeps also two running means of the total power level, over 2 input frames (2 microseconds) and over 2^{20} samples (1.25 ms). If the short-term mean exceeds the long term mean by a programmable factor, the affected frames are considered contaminated by RFI, and optionally flagged. Short and long integration times are fixed in the existing implementation but will be programmable in the final design.
- ***AXI4S LMC Generator***. These modules are responsible for extracting data from the monitored AXI4S streams and packetizing them into SPEAD frames that are further forwarded towards the IO Ring to be transmitted over 1G or 40G network. The main performed tasks are:
  - Reception of data streams from Sample Test Generator, Channeliser and Tile Beamformer.
  - Selection and buffering of requested data according to their specific format and under software configuration.
  - Encapsulation of buffered data into SPEAD packets.

  The resulting SPEAD packets are sent to either the C2C Stream (1 Gb interface) or 40G modules, as streaming UDP encapsulated packets.

  The module is used both for monitor purpose, capturing short snapshots of samples at various points of the signal processing chain, or to send continuous calibration spigots to the MCCS.
- ***AXI4S LMC Spectrometer*** - Integrated Generator. Similarly, to the AXI4S LMC Generator, this module receives AXI4S data streams from Channeliser and Tile Beamformer. Total power data for each spectral channel is computed and integrated for a programmable integration time. Integrated spectra are transmitted as SPEAD packets over 1G or 40G network.
- ***ADC sample capture***. Selects samples from 2 antennas per FPGA, both polarizations, and stores them in a circular buffer in DDR memory, until stopped by MCCS. When stopped, MCCS may access blocks of DDR memory using the control protocol.

5.5.2 Firmware Development Tools

The FPGA firmware development is based on a technology independent approach that facilitates the migration to different devices and vendors. Technology dependent modules are wrapped into common interfaces that abstract the functionality of the involved modules. The tool flow doesn't rely on specific DSP design platforms which would limit the code portability; on the contrary DSP code is the result of manual coding using customizable and re-usable VHDL components.

The following tools are used for firmware development:

1. Vivado provides a complete FPGA tool chain including design entry, synthesis, place and route, bitstream generation and design analysis tools. The Vivado environment is completely scriptable using Tcl/Tk language. The supported Vivado version is 2016.2.
2. ModelSim is a multi-language HDL simulation environment by Mentor Graphics. It is typically used for functional verification of RTL code, although it can also be used for post-implementation simulation of back-annotated models. The latter is not performed routinely due to constraints in simulation speed and required time; nevertheless, it might be used to verify the behaviour of the implementation tools in specific cases. The supported ModelSim version is 10.3c.
3. VUnit is an open source unit testing framework for VHDL/SystemVerilog based on Python language and featuring the functionality needed to realise continuous and automated testing of HDL code. The Vunit framework consists of a Python module and HDL libraries which together implement an interface to the most used HDL simulator. VUnit provides the facilities to drive an HDL simulation from a Python script managing automatically the compilation of the source files and allowing for the parallel execution of multiple test cases. The user can rely on the flexibility of Python language to define large sets of test cases enabling regression suites to be run automatically.
4. In-house developed Python scripts for the generation of AXI4Lite and bus systems register interfaces as presented in section [refer Register Set definition].
5. In-house developed Python scripts for source and project files management and compilation. The set of scripts provides a single push button approach for the generation of the bitstream. This includes gathering of all source files, creation of the register set map and related VHDL code, creation of Vivado project file and bitstream compilation.

5.5.3 IP Block Standard Interfaces

CPLD controls the FPGAs using a proprietary C2C (Chip-to-Chip) bus. FPGA firmware translates read/write requests from the Uniboard Control Protocol to the C2C protocol. The C2C is an address-data-command multiplexed and bidirectional 4 bits bus. A typical C2C MM write transaction is shown in the following figure.

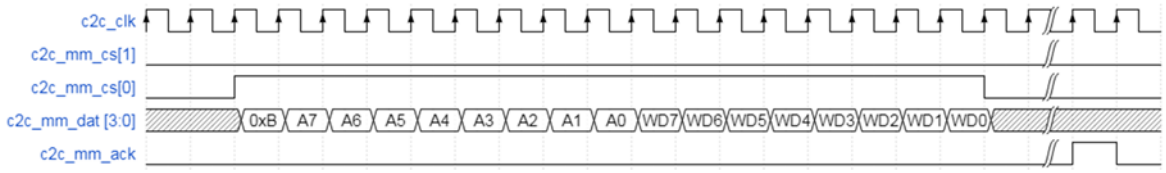


Figure 5-38 C2C Memory Mapped Write Transaction.

To start a write transaction the CPLD asserts one of the two c2c_mm_cs signals selecting the FPGA to address and transmits sequentially the command, address and write data of the transaction serializing them from MSB to LSB over the 4-bit c2c_mm_dat bus. Command word can be either 0xB for a write command or 0xA for a read command. After the last nibble of write data has been transmitted, the CPLD releases the data bus and it waits for the assertion of c2c_mm_ack signal which signifies the completion of the transaction in the addressed FPGA. An example of a read transaction is shown in the following figure.

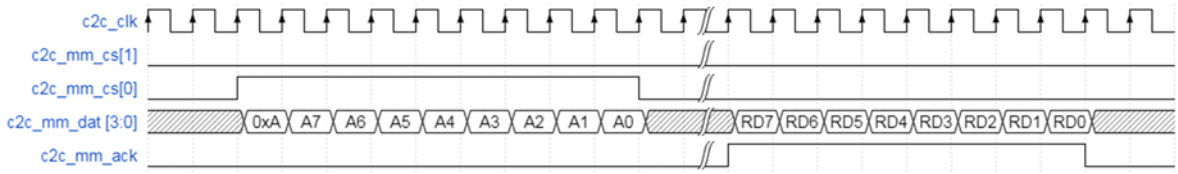


Figure 5-39 C2C Memory Mapped Read Transaction.

All internal FPGA modules are controlled using a subset of the AXI4lite standard bus interface. The interface implements memory mapped slave registers and memory blocks, which are accessed using 32-bit accesses, that are always located at an aligned (multiple of 4 bytes) address.
Internal data communication between modules uses a subset of the AXI4stream protocol. Data handshaking uses the **tvalid** and **tready** signals, and the last transaction in a packet is marked by signal **tlast**. Data samples are packed in the **tdata** field, as a multidimensional array.
Data packet transmitted over the Ethernet interfaces are packetised using the SPEAD standard, and encapsulated into a UDP layer, either in the CPLD or in the multi_udp_core IP block.

5.5.4 Register Set Definition

When developing a complex system where software entities interact with hardware components, it is of primary importance that the relevant information regarding the operation of the hardware is transferred to the controlling software in a consistent way, minimizing the possibility of inconsistency between them.
The principles behind the FW/SW interface model have been kept as simple as possible: a VHDL developer designs a firmware component and defines some memory mapped registers that are accessed by SW to control and monitor the component. In this simple interface model consistency between firmware and software implementations requires that the former exposes a certain number of memory mapped registers and the latter accesses those registers in the intended way.
The information regarding the implemented registers in the running firmware is coded in an XML file, which in fact is used in two ways. Firstly, it is the starting point for the automatic generation of VHDL code implementing the registers interface in the form of an AXI4Lite bus slave. The XML description permits to specify hierarchal 32 bits registers maps down to the single bit level. The generated VHDL code can be directly instantiated by the firmware developer. As the code handles the details of the AXI4Lite bus transactions, the firmware developer doesn't require a prior knowledge of the bus standard.
Secondly, when compiling the FPGA firmware an automated tool-chain gathers all the used XML memory maps and builds a global FPGA XML memory map which is compressed, embedded in the compiled bit file and in turn memory mapped at a specific address. In this way SW can read the implemented memory map directly from the FPGA. The global XML memory map is then used by SW as a symbol table to translate register names into physical addresses; this means that any change in the memory map, such as an address displacement, is transparent to the SW.
The adoption of a consistent memory map format between FW and SW and the use of automated tools for VHDL code generation and for transferring information from FW to SW eliminates the potential for developer-induced errors.
A complete register set definition for the internally developed modules is given in [RD61]. A graphic list of the principal configuration points is listed in Figure 5-40. Signal parameters are highlighted in red, and monitor parameters in purple. Blue lines denote signal monitor paths.

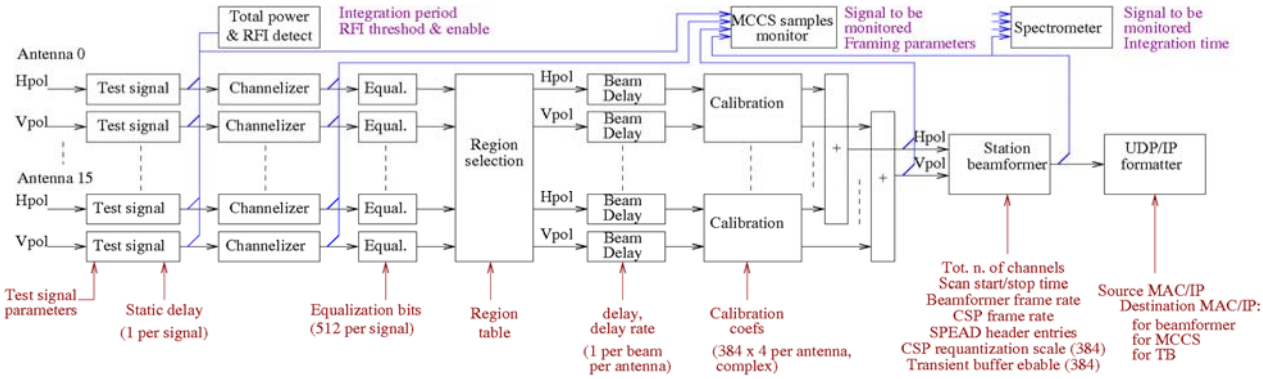


Figure 5-40 Principal configuration points in the signal processing chain

All parameters that are expected to be adjusted during scanning mode can be programmed in advance and associated to a specific time. Time is expressed as a multiple of 256 input frames (or channelised samples), i.e. 276.48 µs. Parameters become active when the specific frame/sample is processed, at the appropriate processing stage.

Static delay is expressed as ADC samples, in the range of ± 124 samples, and is used to compensate for cable length mismatch.

Equalization bits can be considered as an exponent for the calibration coefficients, to compensate for large differences in signal level across frequency channels.

The region table selects up to 16 spectral regions, repeated or not, associated with different beams, substations or simply disjoined frequency regions.

Delay and delay rate are used to reduce the amount of programming for source tracking. A single delay/delay rate value is specified for each antenna and beam, for up to 8 beams. A linear approximation for the delay is sufficiently accurate for about one minute.

Calibration coefficients are expressed as a 2x2 inverse Jones matrix, with complex coefficients. Coefficients are quantised with 16+16 bits, with nominal (unit gain) value of 2^{11}.

The station beamformer is a complex state machine. It generates the packet sequence that will be sent to the CSP. Principal control parameters include start and stop time, total number of processed channels, and packet rate. It generates the SPEAD headers, requiring specification of most parameters contained in the header itself.

The UDP formatter controls the UDP and Ethernet layers of the 40 Gb interface. It receives packets directed to MCCS, CSP and transient buffer, identified using a tag in the **tuser** field of the AXI4s bus. It must be programmed to define the network topology, to determine the TPMs composing a station daisy chain.

Parameters in purple are used to specify monitor functions. All monitor modules can be disabled when not used and synchronised among TPMs.

5.6 Software Components

The software components within the context of SPS can be regarded as device drivers through which commands can be executed and attributes can be modified by the associated TANGO devices running on MCCS. These drivers can therefore be used as interfaces to the hardware itself. This interface takes the form of an API for the TPM, which is used by MCCS but implemented by SPS. For COTS hardware, such as switches, the interface is generally provided by the device itself. This section will focus on the TPM driver, whose associated TANGO device is described in [RD60] Section 6.3.3.

Code development partly follows [RD2]. Good coding practices were followed, using self-documenting code, revision control systems (GIT), adopting guiding styles, Deviations from [RD2] were due to the necessity to have a working system before approval of the standard document, and to the prototype nature of the software itself. Existing software will be aligned to these standards during Bridging.

5.6.1 TPM driver

The TPMs performs all the signal processing in SPS, including signal digitization, channelization, beamforming and data transmission. It primarily consists of a two FPGAs and additional on-board devices, managed by the CPLD. All communication with the TPM happens through the CPLD, which implement the UniBoard Control Protocol (UCP), allowing external entities to read from and write to internal memory-mapped registers.

5.6.1.1 *UCP Protocol*

UCP is a UDP-based protocol which implements a request/reply mechanism for issuing commands and transmitting data between two entities. Due to UDP's unreliability in terms of data loss, where a request or reply packet maybe be lost in transit, a Packet Sequence Number (PSN) is used to be able to map requests to replies. Each request includes a PSN by which it can be identified, and the associated reply packet will include the same PSN. The request packet payload starts immediately following the UDP/IPv4 header. Request and reply packets are identical in this respect: the first 32-bits are the PSN. When a client sends a request packet it will receive the replies, eventually, in a packet which starts with the same PSN. The general packet layout is shown in the top part of Figure 5-41.

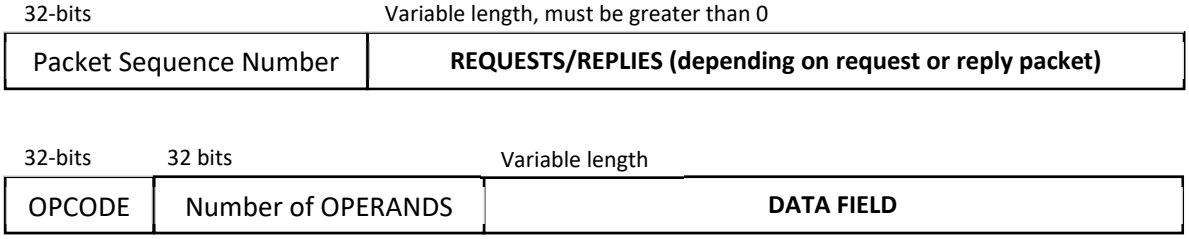


Figure 5-41 UCP request format (above) and packet format (below)

Requests start with an OPCODE field, indicating the requested function. An OPCODE is never 0x0, as it is reserved to mean "end of command sequence". An OPCODE is typically followed by a "NUMBER OF OPERANDS" field, followed by the actual operands, as show in the bottom part of Figure 5-41. Requests including an address adhere to the convention that if the operation was successful, the reply starts with the ADDRESS (optionally followed by the results), or with the binary-not of the ADDRESS in case of detectable failure. All operations on the TPM, including read and writhing registers and memory areas, as well and downloading firmware and programming FPGAs, are performed though two: OPCODES 0x01 (Read) and 0x02 (Write), as shown in Figure 5-42, where a plus between elements in the reply field means that the elements are returned as separate entities in the packet, for example ADDRESS + N * 32-bit Data means that the ADDRESS is returned, followed by N * 32-bit words. In the case where a read-modify-write operation is required, that is only several bits within a 32-bit word need to be changed, three separate requests are required: read the 32-bit word, modify the required bits on the client, write the modified 32-bit word.

The lack of reliability in packet transmission can result in unfavourable actions being performed on TPMs, such as writing to a register twice due to a lost reply packet, resulting in a state-changing operation being performed twice. This is only a problem for a write request, since if a read request fails it can simply be repeated.

OPCODE	0x1	
Command	**Read**	Read N consecutive 32-bit locations starting at START ADDRESS
Argument 1	N (32-bits)	Number of 32-bit words to read
Argument 2	32-bit START ADDRESS	Start address
Replies	ADDRESS + N*32-bit Data	Success. START ADDRESS followed by N*32-bits
	NOT ADDRESS	Failure

OPCODE	0x2	
Command	**Write**	Write N consecutive 32-bit locations starting at START ADDRESS
Argument 1	N (32-bits)	Number of 32-bit words to write
Argument 2	32-bit START ADDRESS	Start address
Argument 3	N*32-bit DATA	Data to write
Reply	ADDRESS	Success
	NOT ADDRESS	Failure

Figure 5-42. UCP read and write opcodes

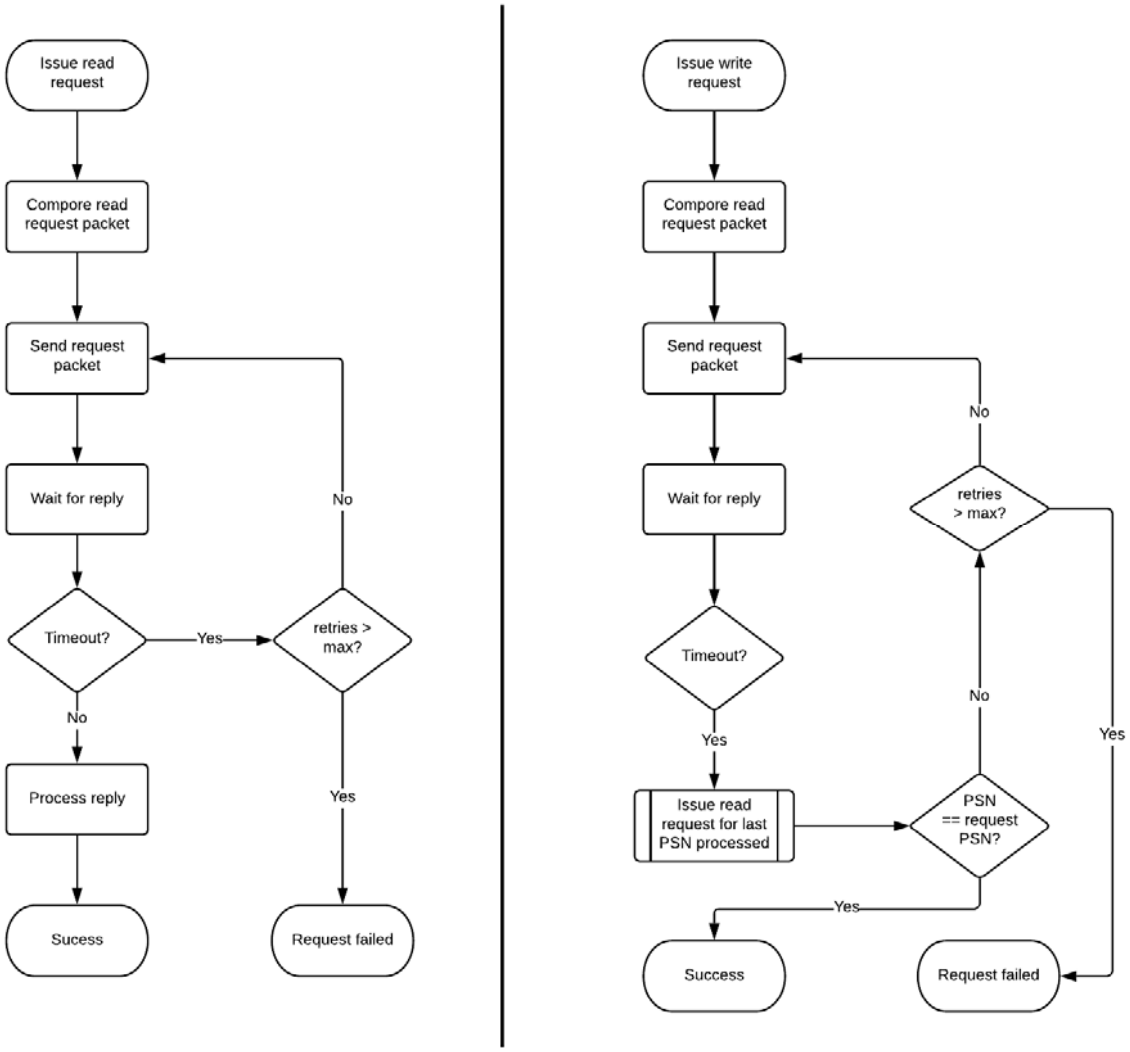


Figure 5-43 UCP read and write request flowchart

Figure 5-43 shows a simple reliability mechanism which can be employed to avoid duplication of write requests due to missing reply packets. It assumes that the TPM keeps track of the PSN number of write requests it processes. With this assumption, when a write request fails on the client, that is, a timeout for the reply packet is reached, a read request for the last write PSN if performed on the TPM. If the PSN matches the write request PSN, that the request was processed, and no further action is required (lost reply packet). If it does not match, then the write request must be re-issued (lost request packet).

5.6.1.2 *Firmware memory map*

Since UCP deals with memory addresses, register mnemonic to address conversion must be performed on the client side. An XML file describing the register list for a firmware implementation is automatically generated during compilation. This bitstream is compressed and catenated to the end of the bitstream. When an FPGA is programmed with a bitstream, the compressed memory map is read by the client (using a series of read requests) and interpreted. The memory map of the CPLD firmware must also be loaded, which is located at a specific address in the memory map. The location and size of FPGA firmware memory maps depends on the size of both the bitstream and the memory map, and these values can be acquired from specific addresses as well.
The XML files provide a mapping between register and memory block names/mnemonics to memory addresses on the board. Three XML files are required, one for the CPLD firmware itself, and one for the firmware loaded on each FPGA (which can be the same for both FPGAs). The registers in a firmware map are logically split into components or blocks (such as channeliser, beamformer, calibrator ...), and in turn each register can be composed of multiple bit-fields, where disjoint sets of bits have different interpretations in the firmware. For this reason, the XML mapping file is composed of a hierarchy of three nodes (excluding the root node):

- **Component node:** Registers are grouped into components, which makes it easier to logically partition the functionality of these registers. For example, registers belonging to different firmware components can be grouped into different nodes at this level. A base address can be specified for each component.
- **Register node**: Each component can be composed of multiple registers or memory blocks, each requiring an identifier (the name or mnemonic) and the memory mapped address. Additional attributes can also be specified, such as the size in words, access permission, the bitmask and a description.
- **Bit node:** A register can be composed of a combination of multiple bitfields. These bitfields are specified in the fourth node level, having an entry for each bitfield in the register. A bitmask per bitfield must be specified.

Figure 5-44 provides a very concise example of an XML mapping file. Each of the node attributes are defined as follows:

- **Id**: The register, memory block or bitfield name/mnemonic. This does not need to be unique within the XML file (such that the same firmware can be loaded on both FPGAs). The IDs of successive levels in the hierarchy are combined to generate the full qualified name
- **address**: The memory address to which the register is mapped. A base address can be specified at all levels (except bitfields). In this case, successive base addresses are added together to form the final address.
- **permission**: Access permissions for the register or memory block. Allowed entries are `r`, `w` and `rw`.

- **size:** The size in words of the register or memory block. If this value is not specified, then the register is assumed to be of size 1 (32-bits). Memory blocks can essentially be defined by setting this value. Note that if a bitmask is specified for a memory block with size greater than 1, then it is applied for all consecutive words.
- **mask**: The bitmask to be applied to the values after reading from or before writing to the memory address.
- **description:** A textual description for the register

```
<?xml version="1.0" encoding="ISO-8859-1"?>
    <node id="rev" address="0x0" mask="0xFFFFFFFF"
        permission="r"
        description="Revision register"/>
    <node id="fpga_id" address="0x4" mask="0x00000001"
        permission="r" hw_rst="no" hw_permission="w"
        description="FPGA identifier"/>
    <node id="reset " address="0x10">
       <node id="adc" mask="0x00000001" permission="rw"
            description="ADC clock domain reset"/>
        <node id="dsp" mask="0x00000002" permission="rw
            description="DSP clock domain reset"/>
</node>
```

Figure 5-44 XML memory map description example

Additional node attributes can be present in the XML file which might be used, for example, during bitstream generation. These should be ignored by the client parsing the file.

5.6.1.3 *TPM driver implementation*

The TPM driver should implement the API defined in [RD61]. This API ensures that different implementations of the driver, or even different versions of the TPM, can be used without required the client code to be changed. It abstracts the features provided by the board and functionality provided by the firmware to high level commands, including:

- General functionality to connect, disconnect, initialise and program the TPM
- Sensor related functionality, so add temperature, voltage, current and ADC RMS can be read
- Timing related functionality to allow for synchronisation across TPMs. These include function to the set and get the NFS time on the TPM, as well as a blocking function to wait for a PPS edge
- Register related functionality, allowing the client to read the interpreted memory map and issue direct calls to read and write registers and memory addresses
- Network related functionality which provides the capability of configuring the network interfaces on the TPM, allowing the formation of the beamforming chain and transmitting the station beam to CSP
- Observation related functionality, including functions for setting truncation scales, setting beamforming regions, downloading calibration coefficients, pointing delays and channel scaling factors to the running firmware
- LMC data related functionality, so that TPMs can be instructed to transmit data to the MCCS servers to be used for calibration, bandpass flattening and diagnostics

5.6.2 Device management

Apart from TPMs, SPS is composed of additional hardware devices which require monitoring and control. For each device type there exists a TANGO device class in the MCCS software architecture.

[RD60] SPS participates to the definition of the operational state of each LFAA element, by exposing a set of monitor points in each sub-element, and by providing a limited health monitor capability. MCCS determines the element operational state based on these information (L3-125). Section 6 describes the monitoring points and commands required for each hardware component, summarised below. The RMB and SMB continuously monitor general health parameters (currents, voltages, temperatures) of the elements under their control, report a summary to MCCS when queried, issue a warning to MCCS and perform safety related tasks when these parameters exceed their safe region.

5.6.2.1 *APIU*

The control interfaces of the APIU is connected to a Subrack Management Board. Each APIU provides the current generated by the connected antennas, as well as internal temperature, voltage and current. Commands for powering up and down specific antennas are also available. The Subrack Management Board acts simply as a proxy, where control packets are sent by the MCCS and forwarded to the appropriate APIU by the switch in the Rack Management Board. The specific protocol which to be used as well as a detailed description of the available functionality is described in [AD34]

5.6.2.2 *Subrack Management Board*

The Subrack Management Board provides a backplane for connecting and managing multiple TPMs with a sub-rack. It acts as a distribution board for power, network and other signals such as PPS. Since it distributes power, it allows for control of power output to the TPMs and exposes the functionality to remotely switch on and off TPMs, as well as provide measured power consumption. Apart from TPM-related functionality, the board itself needs to be monitored and controlled, such that temperature as well as voltage and current use of the board are exposed. The SMB provides however some safety related functionalities, switching off any component in the Subrack which exceeds predefined safety margins (overcurrent, overvoltage, temperature), even in absence of a reliable connection with the MCCS. Monitor and management resources available in the SMB are described in [RD84]. Protocol to communicate with the board is TBD.

5.6.2.3 *Network Switch*

The switching network forms the communication backbone of SPS, and transports both beamformed as well as LMC data. A single switch is responsible for one station, such that it provides a single point of failure for a specific station (an entire rack can also potentially go offline, due to a faulty cabinet power supply for example, however a switch can become unusable through invalid configuration as well, which is within the remits of MCCS). Additionally, switches require potentially complex configurations which should be automated such that when faults occur, and switches need to be replaced, they don't need to be configured manually. The default and specific configuration for switches is stored in the Hardware Configuration Database on MCCS. Apart from this, due to the expected long lifetime of the SKA, it can be expected that onboard firmware and OS upgrades will become available, which should be applied. This process is described in [RD62] Section 6.
The protocol to be used to communicate with the network switches will be defined by the specific switch procured, however it is assumed that the following monitoring and functionality will be available:

- General network configuration, such as definition of MAC tables and DHCP (if required)
- Interfaces-specific configuration, such as setting the MTU and resetting packet counters
- General monitoring, such as reading switch and interface sensors and health
- Interface-specific monitoring, such as reading packet statistics

5.6.2.4 *Cabinet*

The Cabinet is considered as a single TANGO device in the MCCS software architecture. Specifically, it is represented as a TANGO Group device, which contains other devices as members. In this respect, the Subrack Management board is a group device as well. The cabinet device hierarchy is show in Figure 5-45 (note that there are three since it assumes a single 1 GbE switch for cabinet-level monitoring and control, to be used to control power supplies, 100 Gb switches and other devices.) Additional cabinet-support devices, such as power supply units and cooling devices, are control by the SPS Cabinet device itself. Protocols and functionality for these devices is TBD. For a description of how TANGO group devices and TANGO hierarchies operate, and how they are used in the MCCS software architecture, refer to [RD60] Section 4.4, whilst for a detailed description of the monitoring and control functionality of the Cabinet device refer to [RD60] Section 6.3.7

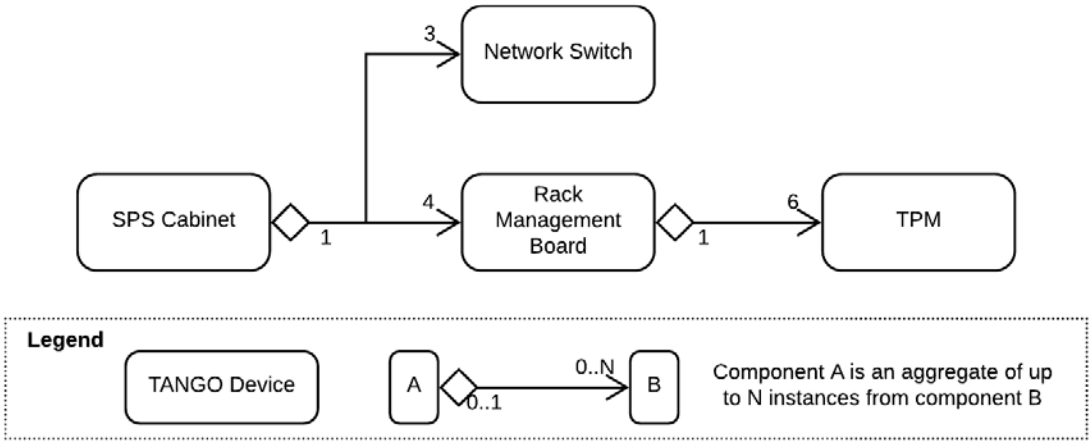


Figure 5-45 TANGO device hierarchy for SPS cabinet

5.6.3 Observation management

Observation creation and management is a complex task which requires the interaction of most of the software components in the MCCS software architecture. When TM issues an observation configuration, the required TPMs belonging to the required station and programmed, initialised and configured (if required) and the beamforming chain is formed. On the MCCS servers the DAQ, calibration, pointing and transient buffer processes are started and configured. Once configuration is complete, the station beam output to CSP is started, whilst on the MCCS server's calibration and pointing start generated the required coefficients. The observation is monitored until TM instructs MCCS to abort or stop the observation. Refer to [RD62] Section 4.1 for a high-level description of the steps required to create an observation, while [RD60] Section 5 goes into much more detail of how this is performed in the MCCS software infrastructure.

6 Dynamic View

The SPS signal processing chain is described in detail in [RD15] with individual modules described separately, [RD79] (Tile beamformer), [RD80] (station beamformer). Its performance has been evaluated both using analytic tools, and by numeric simulation [RD81]. When possible, the TPM 1.2 version has been used to measure these performances on the field.
In the following sections, references to the relevant SKA1-LFAA-SPS_REQ-xxx will be indicated as (L3-xx), and referenced in the requirement traceability matrix in Appendix A.

6.1 SPS Data Flow

Table 6-1 lists all the SPS data flow, with data rates

Description	Source Entity	Destination Entity	Interface Type	Protocol	Data rate
RF analogue signal	FN	SPS.TPM	RFoF optical	WDM analogue	2x400 MHz
Calibration spigot	SPS.TPM	MCCS	40 Gbe QSFP+	UDP - SPEAD	7.6 Gbps /station
Partial tile beam	SPS.TPM	SPS.TPM	40 Gbe QSFP+	UDP - SPEAD	22.8 Gbps /TPM
Station beam	SPS.TPM	CSP	40 Gbe QSFP+	UDP - SPEAD	11.4 Gbps /station
Transient buffer	SPS.TPM	MCCS	40 Gbe QSFP+	UDP - SPEAD	3.0 Gbps /station (peak)
Calibration parameters	MCCS	SPS.TPM	1Gbe	UDP-UCP	< 50 Kb /station
Configuration parameters	MCCS	SPS.TPM	1Gbe	UDP-UCP	1 Mb /station
Monitor parameters	SPS.TPM	MCCS	1GbE	UDP-UCP	0.4 Mb /station

Table 6-1 List of SPS Data Flows

Data rate has been computed with the following assumptions:

- ***Calibration spigots***. Contain samples for one coarse channel at a time, all antennas and polarizations, using the SPEAD over UDP packet format. SPEAD, UDP and IP overhead is negligible (about 1%) and has been omitted for simplicity. This data rate is given by:

$$Antennas * Polarisation * Channel\ Bandwidth(MHz) * Sample\ size(bits) * oversampling$$
$$= 256 \text{ x } 2 \text{ x } 0.781 \text{ x } (8+8) \text{ x } 32/27 \approx \mathbf{7.6\ Gb/s}\ \text{(per station)}$$

- ***Partial tile beams***. All TPMs send and receive a beam data stream using the SPEAD over UDP packet format. The data rate of the partial beam stream is given by:

Bandwidth (MHz) * Polarisation * Sample size * Oversampling
= 300 x 2 x (16+16) x 32/27≈ **22.8 Gb/s** (per TPM)

- ***Station beams***. Final TPM sends a data stream to CSP, the SPEAD over UDP packet format. The data rate of the partial beam stream is given by:

Bandwidth (MHz) * Polarisation * Sample size * Oversampling
= 300 x 2 x (8+8) x 32/27≈ **11.4 Gb/s** (per station)

- ***Transient buffer***. Final TPM sends a data stream to CSP, the SPEAD over UDP packet format. As packet size is smaller, overhead is computed explicitly. The data rate of the partial beam stream is given by:

Bandwidth (MHz) * Polarisation * Sample size * Oversampling * overhead
= 150 x 2 x (2+2) x 32/27x 1.05 ≈ **1.5 G*b/s* (per station, mean)**
= 300 x 2 x (2+2) x 32/27 x 1.05 ≈ **3.0 G*b/s* (per station, peak)**

Peak value corresponds to transmitting the whole band, as packets for TB are generated immediately following packets for CSP.

- ***Calibration parameters***. The MCCS calculates calibration coefficients for each antenna and coarse frequency channel every calibration cycle, nominally 600 seconds but possibly faster. Conservatively, we assume a calibration cycle twice as fast (300 seconds). Each channelised stream form one antenna requires 4 complex coefficients, representing the inverse of the Jones matrix, with each coefficient represented as a 16+16 bits integer. Coefficients are sent over the LMC connection to the FPGA access layer in blocks of 192 32-bits values, and the resulting overhead due to the UDP layer and the UCP protocol is about 20%. The data rate to one station is given by:

  Channels * Antennas * Polarisations * Coefficient size * overhead / cycle length
  = 384 x 256 x 4 x 32 x 1.20 / 300 = ***50 kb/s (per station)***

  The delay and delay rate are provided separately, every 15 seconds, as a single delay and delay rate per antenna and per beam (up to 8). Each delay and delay rate are specified in a 32-bit word. Values are provided in blocks of 16 32-bits values, resulting in an overhead factor of 3.34. The data rate to one station is given by:

  Antennas * Beams * Coefficient size * overhead / cycle length
  = 256 x 8 x 32 x 3.34 / 15 = ***15 kb/s (per station)***

  Using multiple beams and/or substations do not increase the number of calibration coefficients, as each beamformed channel always corresponds to a single beam and/or sub-station.
- ***Configuration parameters.*** During initial setup, in addition to the above, about 500 registers must be set per TPM, or 8000 per station. Setting a single register requires two UDP whole packets, resulting in a very high overhead factor of 42. From previous calculations, calibration coefficients require 15 Mb/station, plus 0.23 Mb for the delays. It has been assumed that the initial setup per station is less than 2.5 seconds, to allow for a MCCS server to configure 8 stations in less than 24 seconds (L3-188). Total data rate to one station is given by:

  (Calibration bits + (Control registers * TPMs * Register size * Overhead)) / setup time
  = (15.2 M + (500 x 16 x 32 x 42)) / 2.5 = **10 Mb/s (per station)**
- Monitor parameters. Data requirements for monitoring each TPM is of the order of 64 words for total power and RFI monitoring, to be read every few seconds, and about the same number of monitor points to be read every minute. Autocorrelation spectrum consists of one spectrum (384 points) per antenna per calibration cycle. Communication overhead is 42x for individual registers, and about 1.2x for spectrum. All registers and spectral data points are read as 32-bit quantities. Total data read is 45 kb/s per TPM, or **0.56 Mb/s per station**.

6.2 Analogue processing and Analogue to Digital Conversion

6.2.1 Analogue receiver, signal conditioning

In the receiver, the PREADU converts the optical RX signal back into an RF electrical signal and perform further signal conditioning (filtering and amplification) prior to the analogue to digital conversion.
A 5-bit digital step attenuator 0-31dB (0.5dB resolution) allows to set the signal to right power level prior to ADC.

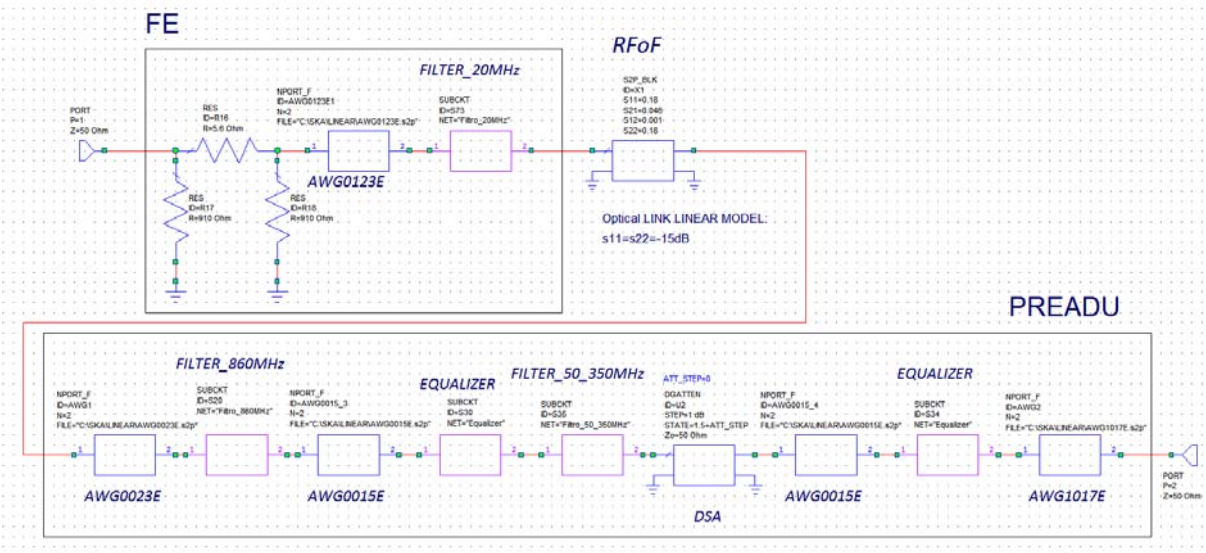


Figure 6-1 MWO schematic single channel RX chain

The RX simulations of the current design/implementation have been performed using MWO/VSS. Further it allows high level block simulations to be carried out not only for the cascaded parameters such as Gain, NF, IP2/3 and P1dB, but also to compute harmonics and intermodulation products present in the receiver output spectrum. This makes it possible to check both the dynamic range for the in-band RFI (IP2 and IP3) and the required out of band rejection at the front-end level due to low frequency RFI. This tool has been used to compute inter-modulations/ harmonics products for signal model analysis. [RD57]

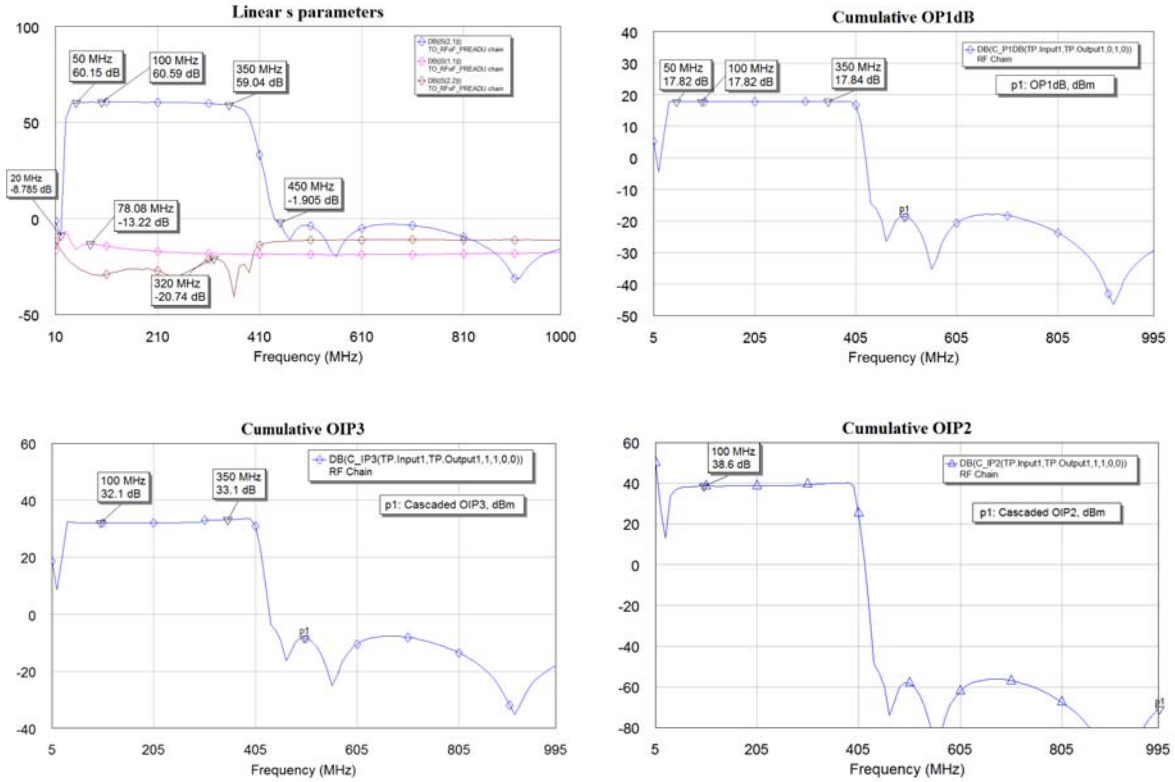


Table 6-2 Summary of the entire RX chain simulation (S parameters, OP1dB, OIP3, OIP2)

Some details are reported on [RD65].

6.2.2 Analogue to Digital conversion

The preconditioned analogue signals are converted to a digital representation using Analogue Device AD9695 dual 14-bit Analogue-to-Digital converters. Each ADC converts signals for the two polarization of one antenna. Samples are transmitted to the signal processing FPGA using a serial JESD204 interface. The AD9695 has a quantization noise of about 9.7 equivalent number of bits (ENOB) over the signal frequency range. Due to limited interface speed, only the 8 most significant bits of each sample are transmitted. This slightly degrades the added noise of the conversion process, to about 7.93 ENOB, i.e. very close to the quantization noise for an ideal 8-bit ADC (L3-174).
Signal is adjusted to an RMS level of about 10-20 ADC units, i.e. -29 to -23 dB below the full scale of the ADC. To avoid clipping for a Gaussian noise, the signal level must always remain below 35 ADC units. This provides a margin of 10 and 4 dB respectively, so to avoid potential problems due to mild RFI it is advisable to remain at the low end of this range (L3-175).
Quantization noise is flat in frequency. The received signal, however, has a strong frequency dependence, due to the intrinsic sky signal spectrum, the presence of RFI, and the receiver response. The actual ADC added noise has been evaluated using a Gaussian shaped noise with the spectrum of the signal at the ADC input, including all these elements. This signal has been processed using a LFAA digital chain model, both with and without the quantization due to the ADC, and the difference has been computed as a function of the frequency and of the input signal level. Result is shown in Figure 6-2, for input RMS level ranging from 12% to 25% of the maximum ADC level (15 to 32 ADC units). Added noise is maximum at the high end of the received band, where the sky signal is lower, and is always below 1%. For an input level of 10 ADC units it exceeds 1% for frequencies above 300 MHz.

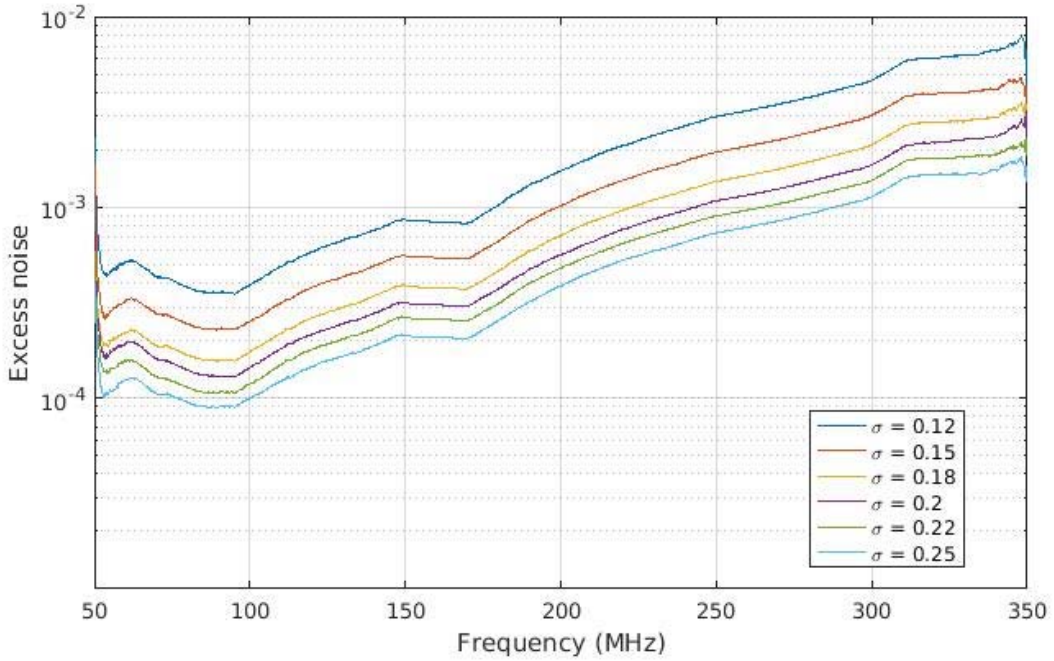


Figure 6-2 Fractional excess quantization noise for input RMS level of 12% (15 ADU) to 25% (32 ADU) of the ADC range

Signal level must be adjusted to reflect diurnal variation of the sky emission and to limit RFI contribution but should not be varied within a calibration cycle.
The ADC introduces intermodulation products, both in its input analogue section and due to the quantization process. The intrinsic linearity of the ADC is specified as an IP2 of about 70 dBFS. In normal operations individual RFI signals represent a fraction of the -25 dBFS digitised signal, and the harmonics are thus suppressed by at least 85 dB, and usually more than 90 dB, with respect to the RFI

fundamental frequency. For strong RFIs, increasing the signal level to 30 ADC units (-9.5 dBFS) harmonic suppression is about 80 dB. Quantization of a noise like signal is a very linear process, for an RMS signal level up to about 28 ADC units (22% of the maximum ADC level). 3rd harmonic is the dominant term for higher signal levels and is suppressed by -75 dB for a signal level of 32 ADU. Above this signal level, it increases quickly.
In conclusion RMS signal level must be kept above 8-10 ADC units, to limit the added quantization noise in the upper portion of the band, and below 30-32 ADC units, to limit harmonics and intermodulation products (L3-203).

6.3 Channelisation and band selection

SPS participates to the channelization of the radio signal, which is shared among LFAA and CSP. The LFAA band is divided into coarse channels in the TPM, which are further channelised to the required spectral resolution in the CSP. Channelisation performance must be analysed considering both elements, for all the CSP operating modes (imaging, zoom mode, PSS and PST beamforming). Final channelization must be uniform, without gaps at the coarse channel boundaries, implying that coarse channels must have a bandwidth larger than the channel spacing, and have a flat response in the non-overlapping region.
Total beamformed region is 300 MHz. In the basic observation mode this corresponds to the LFAA observing band, 50 to 350 MHz, but observed bandwidth can be traded for number of different pointing directions, sub-stations and/or zoom regions. Each pointing direction (beam) may have the same, or different, overlapping or non-overlapping observed frequency region, and different substations may have different pointing directions and/or different frequency ranges.

6.3.1 Number of frequency channels

The number of frequency channels (L3-221) in the first stage channeliser determines the phase accuracy of the fractional delay reconstruction. For a station composed of uniformly distributed antennas in a disk of diameter D, the total decorrelation loss L at the edge of a channel of width δf is $L = \frac{(\pi \delta f d_{max})^2}{4}$ where $d_{max} = \frac{D cos(el)}{2c}$ is the geometric delay at the station's edge. For 512 equispaced channels, $\delta f = 781.25$kHz, and a station diameter of 40 m, the maximum decorrelation is 0.67%, or 0.029 dB, about 2/3 of the total budget of 1% for signal processing. A station diameter of 45 m corresponds to a decorrelation of 0.85%, but this will occur only for a fraction of the antennas and stations, and the total average decorrelation will be closer to the previous value than to this upper limit. The average decorrelation depends on the actual antenna configuration but will be likely around 0.7%. At 45 degrees elevation (the maximum zenith angle for normal observations) the decorrelation is halved, to about 0.43% for a 45m station and 0.3% for a nominal 38m station.
A decorrelation may occur also if there are significant group delay differences among individual antennas in the receiver path, of the order of a few 10 ns, but this would be compensated in the static delay correction module.

6.3.2 Overlapping in the channeliser stage

In a dual stage filter bank the input band is first divided into coarse channels, and then each coarse channel is divided into fine channels. Both coarse and fine channels are resampled at a reduced sample rate, to keep the amount of information almost constant. The edge of each coarse channel is then affected by aliasing from adjacent channels, and if the input of the channeliser is a real quantity the aliased signal has also conjugate phase, producing a large phase error in the measured cross spectrum.

It is thus necessary to provide some guard space at each coarse channel edge that depends on the steepness of the channel filter response.

Fine channels that fall in the guard space must be discarded and not correlated. A simple way to overcome this problem is to resample the course channelised signal at a slightly higher sample rate, thus extending the alias free region. If the alias free regions of two adjacent channels are contiguous, with an overlap between the Nyquist bands of the coarse channels, no fine channel needs to be discarded. The higher sample rate requires more computations per sample and reduces the final spectral resolution, so it must be kept to a minimum. On the other hand, to produce a small oversampling a steeper channel shaping filter is required, so a tradeoff must be found. Oversampling is performed by moving the input sample block by a smaller number of samples than the FFT block length, and by performing the convolution/FFT processing at a sufficient high clock rate not to lose input samples. The relevant filter quantities are shown in Figure 6-3

The input signal is assumed real, with sample rate f_s and total bandwidth $f_s/2$. The bandwidth is divided into N channels of useful bandwidth, and channel separation, equal to $f_s/2N$. The channelised samples are computed at a higher rate, given by an oversample factor O_f, and the output Nyquist band is thus given by $f_n = O_f f_s/2N$. The filter cutoff frequency is fixed, at half the channel separation, $f_1 = f_s/4N$, while the stop band begins at the frequency $f_2 = f_n - f_1 = (2O_f - 1)f_s/4N$. This is shown in Figure 6-3(left).

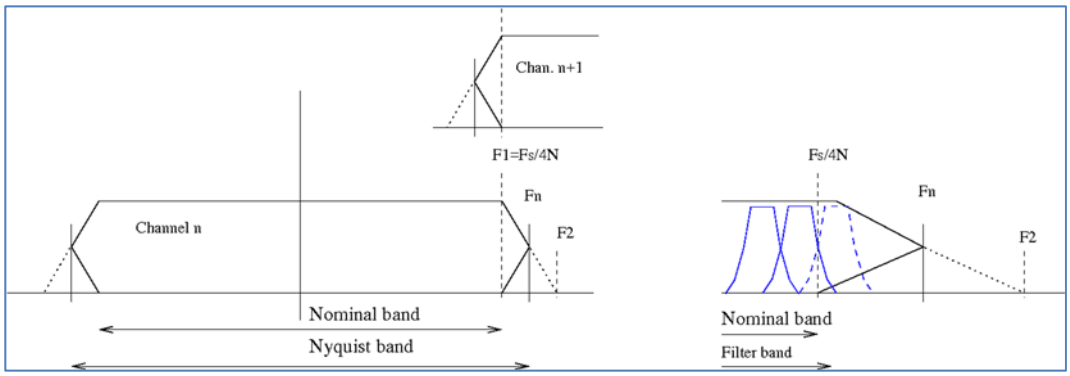


Figure 6-3 Oversampled, overlapping coarse channels

Each channel will be further divided into fine frequency channels in the correlator, using an FFT with several channels that is a power of two. To allow to re-grid these fine channels on a regular grid, the oversampling factor o_f must be of the form $2^n/k$, with n and k integers. Practical values are 32/26 = 16/15, 32/27 and 32/28 = 8/7. We have chosen 32/27 as it provides a good compromise between filter length and increase in the processing requirements (L3-208).

6.3.3 Filter shape and number of filter taps

The second stage (fine) channeliser, in the CBF, uses a band that extends slightly beyond the nominal passband of the first channeliser (coarse channel), due to the finite stopband rejection of the fine channeliser. The SKA1 specifications require that each fine channel response drops to -3dB at the fine channel edge, to -60 dB at the center of the adjacent channel. Therefore, the passband of each LFAA channel must extend to about half the size of the CBF channelisers. For the imaging and PST channelisers this is not a problem, as the number of fine channels per coarse channel is very high. This is not negligible for the PSS fine channeliser, which produces 54 PSS channels over each coarse channel. Moreover, if the channeliser is implemented by a 64-point FFT, the portion of each channel that will be channelised would be asymmetric (from -28.5 to +27.5 PSS channels). It has therefore assumed that the CSP_Low.CBF PSS channeliser upshifts the input signal by 1/128 of a channel, in order to obtain a symmetric set of PSS channels.

To compensate for these effects, the passband of the filter must be slightly extended beyond the nominal channel edge, from 390.6 to 397 kHz.

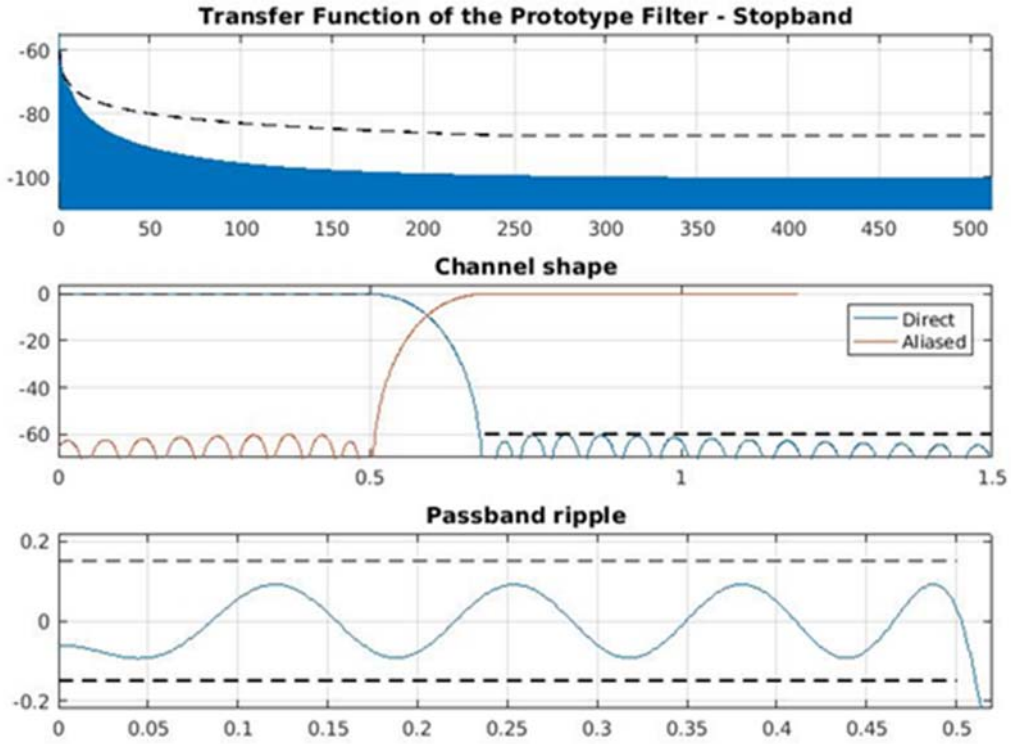


Figure 6-4 Normalised response for filters oversample factor of 32/27

Several possible algorithms can be used to compute the filter response. We used the Remez algorithm aiming at an equiripple response. The Remez algorithm allows to independently select the passband and stopband ripple. The filter has a ± 0.10 dB ripple, and about 60 dB minimum stopband attenuation (L3-181). The algorithm does not converge for more than about 2000 taps, so the filter has been initially computed for a channeliser with 64 channels, and then filter taps were interpolated, using a spline interpolator, to the final number of channels. The procedure produces a non equiripple response, with slightly lower stopband attenuations for the first adjacent channels, and much higher (up to 100 dB) attenuation in the interpolated region. The extra stopband gain is useful in rejecting strong RFI signals. The filter impulse response is symmetric, with an even total number of taps (16384). Filter response is shown in Figure 6-4, compared with the specifications in (L3-182). Filter tap coefficients are represented with 18-bit accuracy, resulting in about 0.5 dB degradation in the stopband rejection with respect to an infinite precision representation (Figure 6-11).

Total uncalibrated passband ripple is constrained to ± 0.15 dB. After channelization in the CSP, which uses a critically sampled PFB with 4096 channels (channel spacing 226 Hz), the ripple present in the passband is corrected multiplying each channel by the inverse of the passband and averaging the channels after correlation to the desired spectral resolution. Total post-calibration passband error is constrained to ±0.01dB, of which half (±0.005 dB) is allocated to the CSP channeliser, and ±0.002 dB to the LFAA-FN (L3-183). To guarantee this error, the spectral slope if the LFAA channeliser is constrained to ±0.003 dB over one zoom imaging channel (226 Hz). The slope for the baseline LFAA filter's bandpass is shown in Figure 6-5

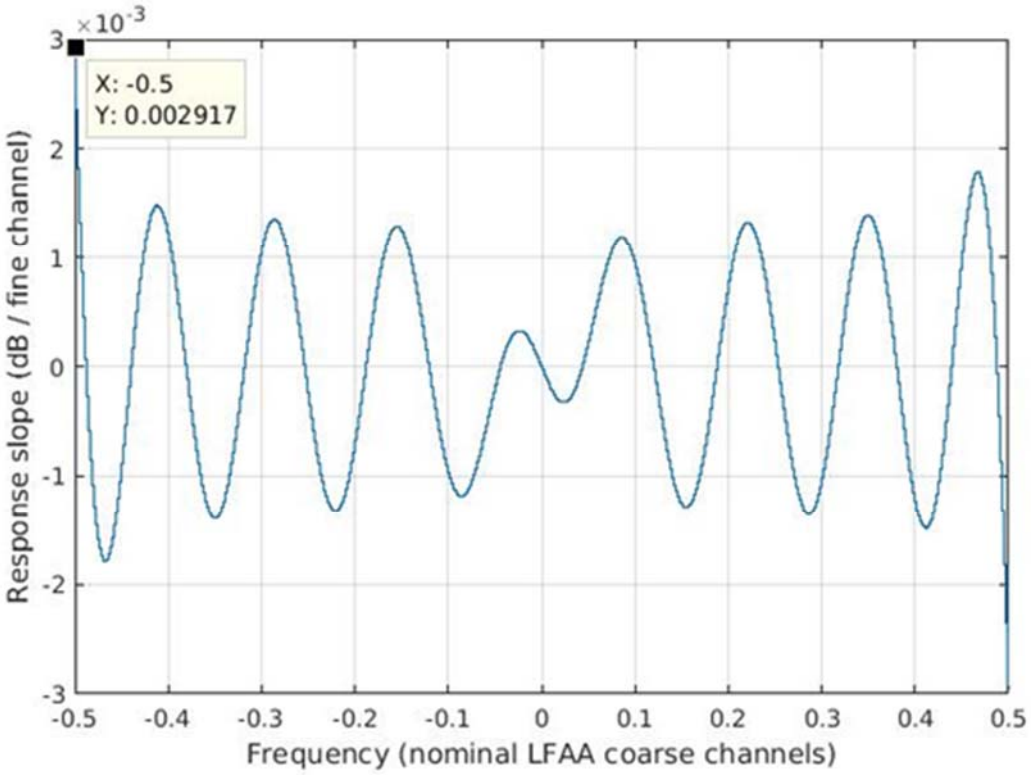


Figure 6-5 Spectral slope across one zoom imaging channel

To cross check the L1 requirement, the composite response of the LFAA filter and a hypothetical 2nd stage filter, after the above procedure, has been computed, and the result is shown inFigure 6-6. The 2nd stage filter response is not optimised and represents a worst-case situation. Left figure is for the whole LFAA channel passband, and right is a zoom over the edge region, which represents the worst case. The total response error due to both filters is limited to ±0.004 dB.

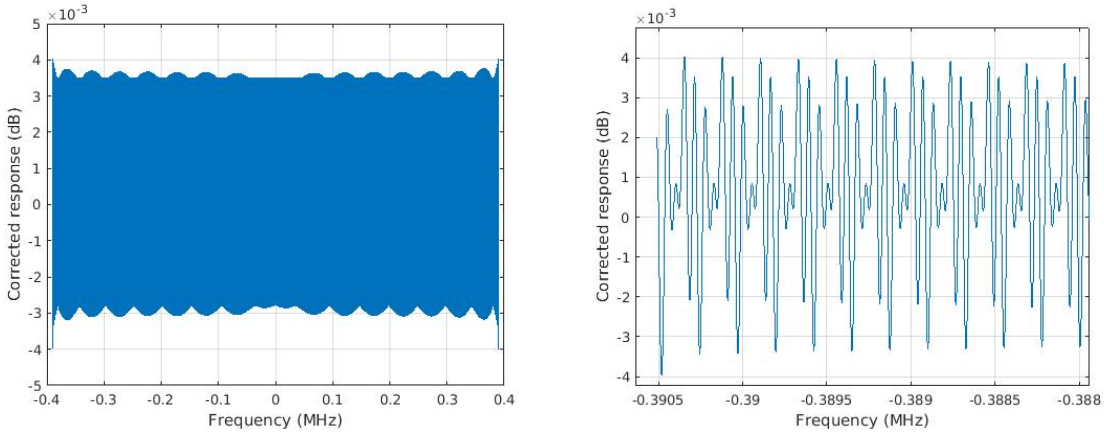


Figure 6-6 Composite spectrum of LFAA channeliser and hypothetical good quality 2nd stage channeliser

The same analysis has been performed for the PSS channeliser. Flatness for this channeliser spectral response is not specified, and has been assumed to be ±1% (0.043 dB). The response is shown in Figure 6-7.

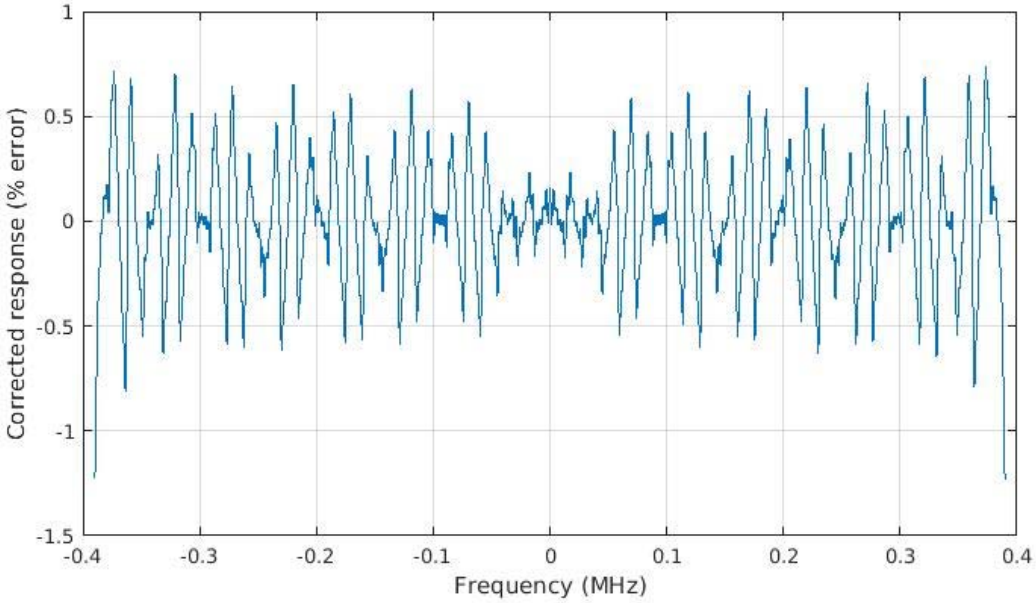


Figure 6-7 Composite spectrum of LFAA channeliser and hypothetical good quality PSS channeliser

6.3.4 Total aliased power

Performance has been measured using a test signal like the one analyzed in [RD57]. It is composed of an uncorrelated shaped noise, with a spectrum that includes broadband RFI emission, and a correlated noise with a power law having the same spectral index of the Galactic synchrotron emission.

Figure 6-8 shows the total aliased noise, and the aliased noise excluding the contribution from an increasing number of immediately adjacent channels. The total aliased noise is slightly more than -60 dB, but most of it comes from the adjacent channels. Excluding 2 channels on each side, the aliased signal does below -60 dB (L3-202). Ignoring more channels in the transition region of the stopband does not improves significantly the situation. A significant contribution comes from the large broadband RFI between 240 and 270 MHz, and the high low frequency sky emission also contributes, for a total aliased signal around -65 dB.

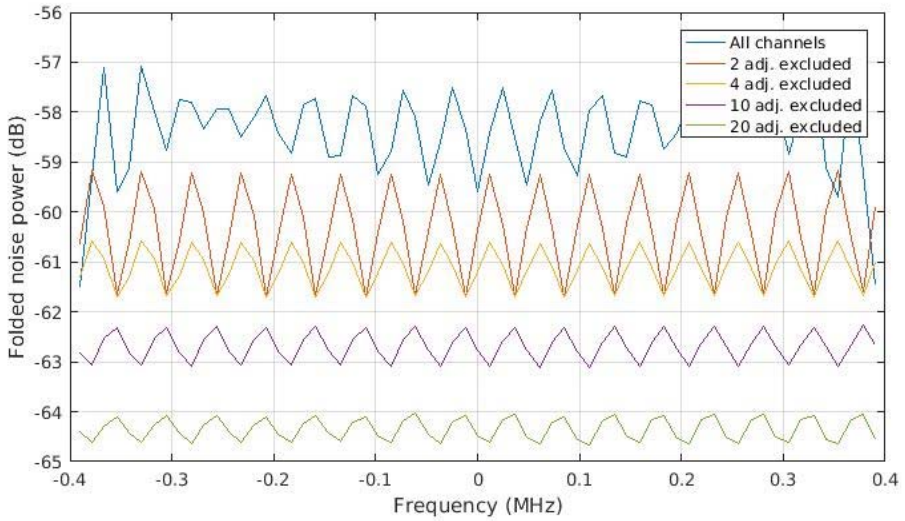


Figure 6-8 Spectral density of the aliased noise, total and excluding a variable number of immediately adjacent channels

6.4 Calibration, Antenna Weight and Polarisation Correction

After channel selection, the samples in each channel/region for both polarizations are multiplied by a complex 2x2 matrix, which include:

- Calibration for the receiver complex gain
- Phase correction for ionospheric calibration
- Correction for the Jones polarization matrix, including rotation of the polarization plane
- Tapering of each antenna for improved beamforming (L3-189)
- An instrumental equalization coefficient, to be removed in the SDP, to optimise the signal amplitude
- Optionally setting the calibration coefficient to zero allows disabling an antenna (e.g. a faulty one) in the beamforming process, or to implement substations (L3-225).

Thus, the beamformed signals S(t, ν, b) for one station, two polarizations, for the frequency channel ν and beam *b* is given by:

$$\begin{bmatrix} S_h(t,\nu,b) \\ S_v(t,\nu,b) \end{bmatrix} = \sum exp\left(2\pi j \nu \tau(t,a,b)\right) \begin{bmatrix} C_{hh}(\nu,a,b) & C_{h\nu}(\nu,a,b) \\ C_{\nu h}(\nu,a,b) & C_{\nu\nu}(\nu,a,b) \end{bmatrix} \begin{bmatrix} A_h(t,\nu,a) \\ A_v(t,\nu,a) \end{bmatrix} \quad (7.1)$$

where the delay is approximated with a linear expansion:

$$\tau(t,a,b) = \tau_0(a,b) + t\dot{\tau}(a,b) \quad (7.2)$$

S(t, ν, b) is the beamformed signal for beam b, A(t, ν, a) is the channelised signal for antenna *a*, τ (t,a,b) is a linear approximation for the geometric delay of antenna *a* relative to beam direction *b*, and C(ν,a,b) is the correction matrix. All quantities, except the delay, are complex, and specified for the 384 selected combinations of frequency and beam directions. The corrections are referred to the centre of each frequency channel and decimated sample interval.

Matrix C is expressed as a complex mantissa, with 16 + 16 bits of accuracy, and a 3-bit exponent. The exponent is used in the FFT equalization stage described in section 6.4.3 and is usually kept constant during an integration. The mantissa is updated at a rate comprised from the integration cycle time (1.8 s) to the calibration cycle interval, currently specified as 10 minutes. Calibration coefficients are calculated by the MCCS. They require 1.6 Mbyte per station that, at the highest update rate, use 2-3% of the network bandwidth.

6.4.1 Substation implementation

Substations (L3-225) are implemented using the beamformer structure described above. Total bandwidth across substations is limited to 300 MHz, and each substation bandwidth must be a multiple of 8 LFAA channels starting at an even channel. Selection of antennas composing the substation is obtained by setting to zero the calibration coefficients of antennas not participating to the substation. An antenna is assigned to just one substation, and the pointing direction (delay and delay rates) can be specified independently for each antenna. Up to 8 beams per substation are available, even f in this case the available bandwidth per beam will be very small. If less than 8 beams in total are implemented across substations, antennas can be assigned to more than one substation.

6.4.2 Tile beamforming

Actual beamforming is performed by multiplying each corrected channel by a complex phase, i.e. the phasor in equation (4.2), and summing over the antennas.

As the delay correction is performed using a phase correction, there is a residual phase error that increases towards the channel edges. For a channel width of 781.25 kHz, a uniform circular station with a diameter of 40 meters and pointing to a zenith angle of 45 degrees (the maximum angle for normal observations), the maximum phase error is 0.12 radians and the corresponding beam decorrelation for a uniform circular station is 0.33%, or 0.015 dB. SKA specifications include a station diameter of up to 45 meters and pointing up to the horizon. In this case the maximum phase error increases to 0.18 radians, and the decorrelation at the band edges is 0.8% (0.037 dB).

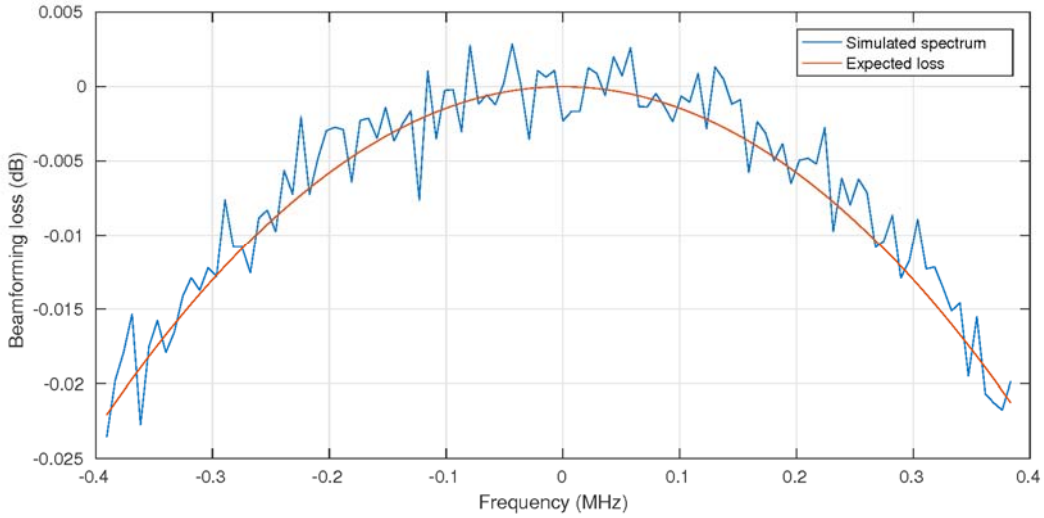


Figure 6-9 Decorrelation due to finite spectral resolution, for a source elevation of 20 degrees and a station of 36m diameter.

Decorrelation is a shift in beam position and refers to the nominal pointing. The global effect on mapping is more complex and can be corrected by considering a frequency dependent beam but decreases the signal-to-noise ratio. This decorrelation model has been tested using a simulated array, with results in

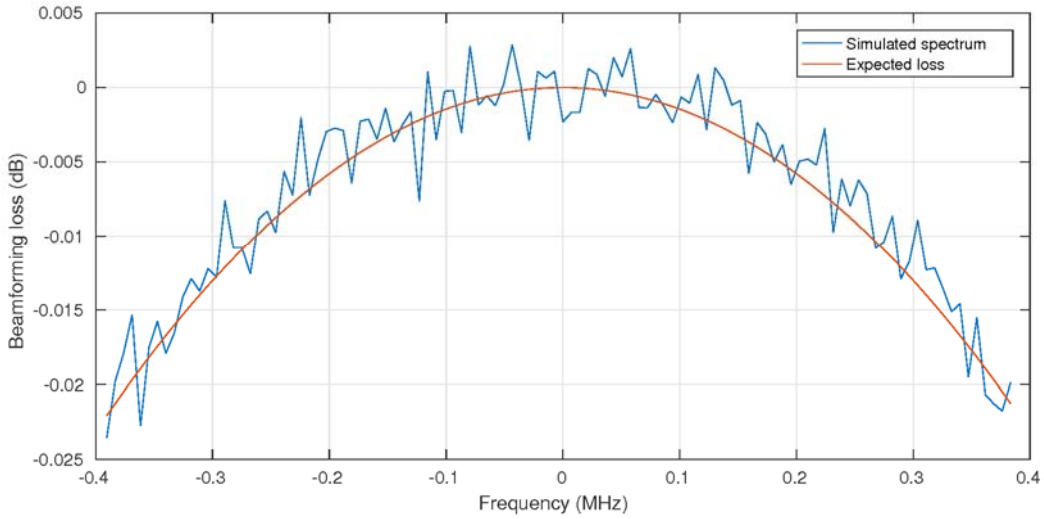


Figure 6-9, for a 36-metre station at 20 degrees elevation.

The delay phasor exp($2\pi j\, \tau(t, a, b)$) is computed internally from a starting delay and delay rate. Linear delay is computed and updated every 1024 channelised samples (1105.92 µs). These quantities, and all the calibration coefficients, are calculated externally to the TPM-ADU, and expressed as integer values. Phase is expressed with a resolution of 4096 steps/turn, delay with a resolution of 153 fs in a range of ±80 ns (±24 m), and delay rate with a resolution of 8.4 fs/s and a range of ±17 ps/s, i.e. up to

3 times the sidereal rate for a station diameter of 45 meters (L2-116). Phase error in the beamforming is specified to be less than 1.7 ps (L3-178), or 0.2 degrees (3.7 mrad) at 350 MHz. For a source moving at a sidereal rate, delay and delay rates can be updated every minute before the phase error reaches this level. An update rate of 15 seconds is enough for data rates up to 4 times the sidereal rate. An example of the phase error is shown in Figure 6-10, for the worst-case sidereal tracking at 22.5 m from the phase centre and 350 MHz sky frequency. The fast sawtooth is due to the finite phase resolution, and the parabolic component to a delay quadratic term of 0.4 fs/s^2. The actual delay error is below 2.5 mrad (1.1 ps). Delay errors tend to cancel in the beamforming sum, resulting in a final phase error of about 10^{-4} rad (L2-209).

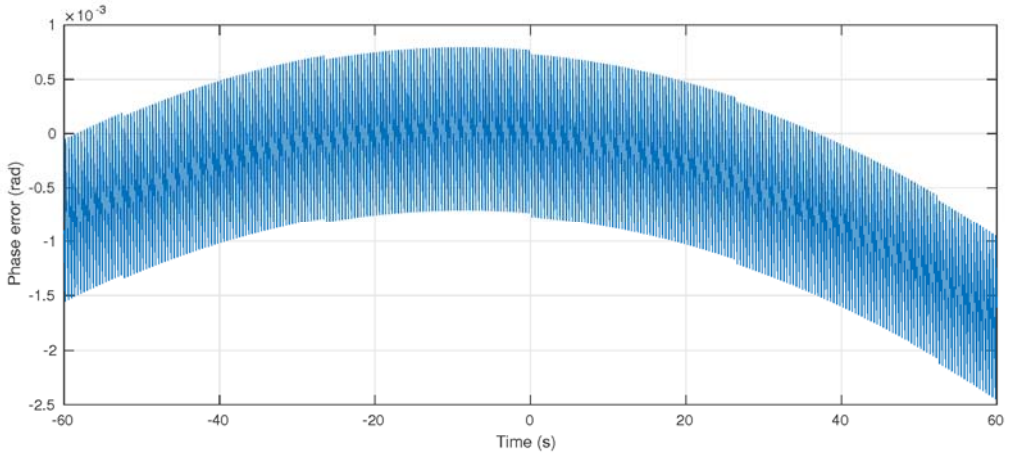


Figure 6-10 Example phase error in the tile beamformer

Both calibration coefficients and delay/delay rates are updated using a double bank scheme. The MCCS updates the coefficients in one bank while the old ones are used from the other. When all the new coefficients have been downloaded, the active bank is swapped synchronously on a specified frame, for all TPMs-ADU. Calibration coefficients are computed every calibration cycle (600 seconds) and transmitted from the MCCS directly to the TPMs using the LMC management network.

6.4.3 Station beamformer

Sum of aligned antenna signals is performed in three steps:

- Each FPGA processes, channelises and beamforms the signals for 8 antennas, 2 polarizations, and 384 frequency channels. These 8 signals are summed together;
- Odd and even channels are exchanged among FPGAs and summed in a tile partial beam. Each of the two FPGAs in a TPM-ADU then processes only the odd, or even, channels;
- Partial beams are stored in a large memory buffer, implemented in DDR memory;
- A travelling packet is formed in the first tile in a station; the packet is composed of consecutive samples for a small subset of channels, and travels across all the tiles in the station;
- Each tile adds the corresponding partial sum to the travelling packet;

The final tile receives the complete station beam and assembles it in the correct format to be sent to the CSP. Calibrated samples are quantised to 16+16 bits. The tile partial sum is quantised to 12+12 bits, after dividing the sum result by 2^7. The travelling station beam samples are represented with 16+16 bits. This prevents any integer overflow to occur during the sum. The final samples are requantised to 8 bits, with appropriate rescaling, before sending them to the CSP.

TPMs are assigned to a station, composed of up to 16 tiles (256 antennas) organised in a chain. The chain is defined in software, by programming the IP address of the next tile in the 40 GBE interface. Due to the network structure, 16 tiles are permanently assigned to a station, and must reside in the same SPS rack, but at runtime less than 16 tiles can be used to form the station.
The station beamformer stores the tile partial beams in DDR memory. Half of the 2 GB memory present in the board is used for this function, reserving the other half to the antenna buffer described in Section 6.7.1 Samples are stored in blocks of 4 spectral channels, 2 polarizations, and 256 consecutive time samples. When 4096 samples have been collected, the first tile in the station chain fetches in turn data blocks from memory, format them into SPEAD packets of 256 samples, 2 polarizations and 4 channels and send them to the next TPM-ADU in the chain. Other TPMs-ADU wait for these packets, fetch form memory the corresponding blocks with the same channels and time interval, sum them together and forward the result down the chain. The last TPM-ADU in the chain reformats the samples to 8 bits, separates the 4 channels and accumulates them into separate packets. When all 8192 samples have been received, the packets are forwarded to the CSP (L3-145).
To reduce the number of high-speed interconnections, both FPGAs share a single 40 GBE port to implement the station beamformer daisy chain. If a packet is received containing channels stored in the second FPGA, the packet is fetched and transferred using the FPGA-to FPGA interconnection. Summing logic and the final buffers to the CSP are present only in the first FPGA.
The SPEAD header for the partial packets contains just the time and channel indexes, to allow for a correct block to be fetched from memory. The final packet to the CSP contains actual time and frequency information, calculated from the above indexes, and other ancillary data, programmed from the MCCS. Subarray definition is embedded in the SPEAD header (L3-223).

6.5 Requantisation stages

The Signal is requantised during processing in several points. Requantisation is performed together with clipping, using the same algorithm for all requantisation operations. To prevent a DC bias, rounding is always performed using a “round away from zero” scheme. This introduces a small level dependent variable gain, inversely proportional to the signal RMS amplitude before the requantisation. Therefore, requantisation is performed sparely and on signals with the largest possible representation.
Signal RMS level after each requantisation must be comprised between 8-10 units to about 25% of the maximum representable number. For signal level below 8 units the added quantization noise increases above 0.1%, contributing significantly to the digital noise budget. For signal levels higher than the above range the quantization introduces a variable compression factor. The corresponding gain error is around 0.02% at the given upper limit but increases very quickly with signal amplitude.
Clipping is used to remove unused bits. For a signal having a Gaussian distribution, occasional outliers are relatively frequent. For a signal RMS amplitude of 25% of the clipping level, clipping occurs about 30 times a second in each spectral channel. This would invalidate a large portion of the data if flagged. Therefore, signal exceeding the representable level are simply clipped if their amplitude is less than twice the representable level and flagged for RFI otherwise (L3-200). In this way flagging occurs only for signals which are effectively affected by narrowband RFI.
Requantisation is performed at the following processing stages:

- In the channeliser polyphaser filter, before the FFT engine, to 12-bit precision
- After the FFT, to 12-bit precision
- After calibration, to 16+16 bits
- After tile beamforming (sum of 16 antennas), to 12-bit precision
- After station beamforming (sum of 16 tiles), to 8-bit precision

Filter calculation is performed using fixed point quantities, both for the samples (8 bit) and for the tap coefficients (18 bits). The intermediate quantities use the correct number of bits to avoid overflow in any situation, resulting in a final sample size of 27 bits. This result is rounded to 12 bits, using symmetric (away from zero) rounding. Total gain of the filter, considering the actual used filter tap coefficients and rescaling, is about 3.55. For a signal at the nominal input level, the RMS amplitude after the filter and at the FFT input is around 69 units, and the maximum possible sample value is 878 units.

The FFT blocks do not perform any intermediate downscaling. The signal width is increased to 18 bits in the first 6 radix-4 blocks, and to 20 in the final complex-to-real stage. No overflow is expected to occur if the signal RMS amplitude is kept below 256 units at the FFT input, or 70 ADC units at the ADC, even for monochromatic signals. If an overflow occurs, the affected samples and channels are flagged. This corresponds to a signal level that would anyway saturate the analogue stages in the receiver.

The FFT output is rescaled to 12 bits. Rescaling occurs by discarding a variable number of bits (1 to 8) and rounding. Number of bits discarded can be programmed for each antenna and spectral channel, to partially equalise the signal level and compensate for the steep spectral slope of the astronomic signal. For typical LFAA operations, discarded bits range from 2 at 350 MHz, to 7 at 50 MHz, with larger values on individual channels affected by mild RFI.

Calibration includes an equalization factor, to keep the tile beamformer sum in the 12-bit valid range. Station beamformer is performed with 16 bits of accuracy. This ensures that the sum of 16 partial tile beams does not overflow 16 bits. Each channel in the station beamformer final stream is rescaled by multiplication to a 16-bit rescaling value, and requantised to 8 bits for the CSP sample stream. RMS amplitude of the samples to CSP is set in the range of 8 to 16 units, for a maximum added noise of 0.15%.

Total requantization noise computed by analysis [RD15] and by numeric simulation [RD81] for the main SPS elements is listed in Table 6-3.

	50 MHz	350 MHz
ADC	0.05	1.1
Polyphase filter	0.01	0.12
FFT	0.00	0.03
Equalization	0.01	0.01
Beamforming decorrelation	0.33	0.33
Beamforming requantization	0.01	0.01
Final CSP 8 bit requantization	0.15	0.15
Total	0.56	1.75

Table 6-3 Added noise due to quantization and beamforming (percent)

Rescaling factors in the channeliser/calibration and in the final requantisation are determined by computing dynamic spectra of the antenna and station autocorrelation spectra.

Transient buffer samples are quantised to 2+2 bits (optionally to 4 or 8 bits). Quantization is performed dynamically, as described in section 6.7, and the requantisation factor used is sent together with the data.

Quantisation of processing coefficients, bot for filtering and calibration, also introduces errors in data processing, and possibly added noise. Filter tap coefficients are represented with 18 bits of accuracy. This guarantees good filter spectral response fidelity to about 100 dB of stopband rejection (Figure 6-11). FFT twiddle factors (sine and cosine tables) are also represented with 18 bits of accuracy. Requantisation of the product is performed after each twiddle factor multiplication, resulting in a final added noise that is about 0.05%.

Calibration coefficients are represented with 16 bit complex. Using a normalization value of 2^{11} for the coefficient gives a calibration accuracy better than 0.1%, or 0.001 radians in phase (L3-209). Errors tend to cancel out in the beamforming sum, resulting in a final error that is about 10 times lower.

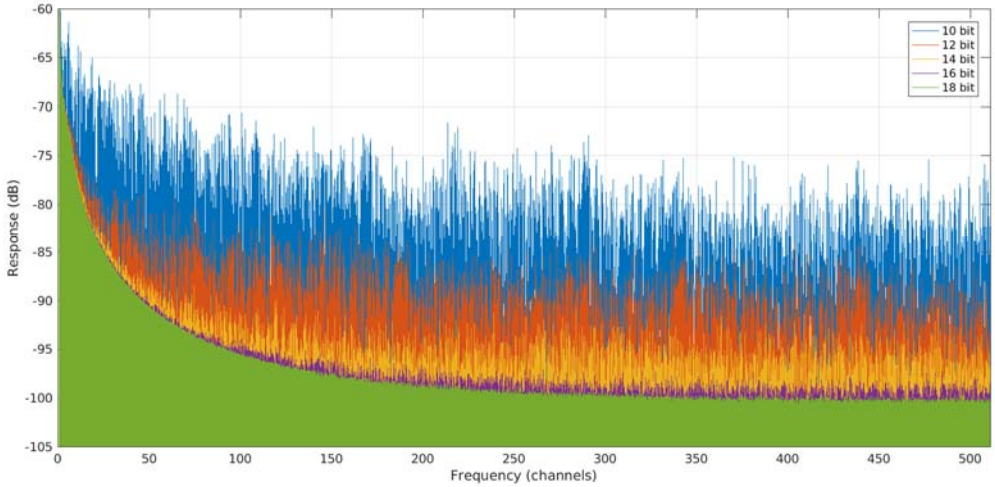


Figure 6-11 Effect of tap coefficient quantisation on stopband attenuation

6.6 FPGA Bitstream Configuration

A single FPGA bitstream is used to provide the intended functionality, FPGAs are configured during initialization and further FPGA reconfigurations are not required while the ADU is on-line.
Bitstream configuration of the ADU FPGAs is performed by transferring the bitfile over the network and commanding the CPLD to write into the FPGAs configuration memory using SelectMap bus. The process can be executed from either MCCS server, Subrack or Rack Management board. In the first case the bitstream is stored as regular file in the MCCS storage area, while in the other cases the bitstream must have been be previously deployed to the Sub-rack/Rack management boards or in the TPM flash storage and written into local non-volatile memory, such that the MMCS is able to command the start of the FPGA configuration process with the Sub-rack/Rack management autonomously transferring the bitstream to the involved ADU over the network. The bitstream file size is about 27 Mbyte, benchmarking showed that a configuration time of less than 1 second is easily achievable. Furthermore, the MCCS server can run multiple FPGA configuration processes in parallel or use broadcast communication to program multiple ADUs at the same time (L3-127). All elements which are programmed using non-volatile memory (CPLD, MCU) can be initially programmed using in-system programming tools (L3-126). Normal update of the associated software/firmware is performed by LMC through the network. In-system programming is used only in the initial production of the boards, and in the unlikely event of corruption of the download code.

6.7 Transient Buffer Storage/ Trigger

SKA1 must capture transient events (L3-213), e.g. fast radio bursts (FRB). FRB detection capability is included in the PSS component of the CSP and may trigger a data capture of a segment of about 500 seconds, that is the expected transit time for a short pulse from 300 to 150 MHz due to dispersion for a dispersion measure of 3000 pc cm-3. The trigger may occur up to 600 seconds after the first sample to be captured has arrived at the LFAA. The captured signal consists in all station beamformed samples for a bandwidth of 150 MHz, quantised at 2+2 bit per sample, complex, dual polarization. 4+4 or 8+8 bit quantisation is also possible, with the limitation that the buffer will capture one every 2, or every 4 (respectively) spectral channels in the selected spectral region.
The buffer is physically located inside the MCCS, and the samples are transmitted from the last TPM-ADU in the beamformer chain after each sample packet is transmitted to the CSP. The packet to MCCS is just a 2 bits version of the same packet, with the requantization scale computed at the optimal level

for each packet and specified in the SPEAD header. Packets of 2, 4 or 8bit samples to the transient buffer (TB) are directly derived from the samples sent to the CSP. The related logic is included in the final stage of the station beamformer, as part of the packetiser/formatter for the CSP interface. A conceptual schematic of the TB and CSP formatters is shown in Figure 6-12.

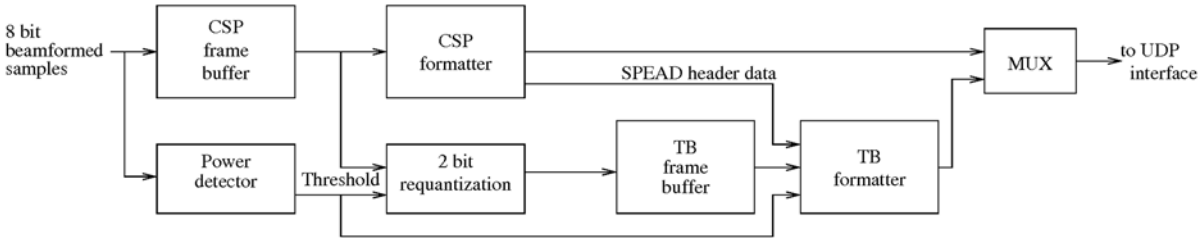


Figure 6-12 Requantisation and packet formatting for samples to the station transient buffer

The samples to the CSP are accumulated in a packet buffer in the station beamformer of the last TPM-ADU of the beamforming chain. Samples arrive to the tile in blocks of 256 samples, and after being requantised to 8 bits they are stored in a buffer to be sent to the CSP in packets of 2048 samples. As they enter the buffer, the amplitude statistics for these samples is calculated for each packet. From that, an optimal threshold for 2 bits quantization is derived. The threshold is different for each packet, to follow the expected fast amplitude variations in the signal level. Threshold calculation algorithm is based on mean absolute value, to avoid the calculation of a square root.
When the packet is sent to the CSP, samples are quantised to 2 bits, using the calculated threshold, and stored in a separate buffer. Elements of the SPEAD header for the CSP packet are also saved, to be reused in the SPEAD header for the TB packet. After the CSP packet has been sent, the TB packet is also sent, with a SPEAD header containing mostly the same information (time tag, frequency channel, beam, station, etc.) plus the value used for the quantization threshold. The CSP packets are sent at an approximate duty cycle of 30% over the 40 GB Ethernet interface. The TB packets are about ¼ the size of the CSP packets and can be safely transmitted just after the corresponding CSP packets, without interfering with the transmission of the next CSP packet. The UDP formatter selects the destination address of the two packets according to ancillary information specified alongside the packets.

6.7.1 Antenna sample transient buffer

Some custom experiments require access to the raw channelised samples for a subset of the antennas. This capability is currently proposed as ECP, but the possibility to capture raw ADC samples is anyway extremely useful for debug purposes.
The buffer selects a subset of the ADC data streams. Each of the 2 FPGAS select 2 of the 8 ADCs, in both polarizations, at the full sample rate. These streams are stored in the local DDR memory, at an address that corresponds to the physical arrival time modulus the buffer size. Current DDR memory size allows for a few 160 ms of data to be stored, assuming half of the memory is to be used for this purpose.
When a trigger signal is received the buffer is frozen and the memory can be accessed using the control interface. Read-back speed is limited by the low bandwidth of the control interface, but typically only a few milliseconds of data will need to be read.

6.8 RFI Detection and Flagging

The SPS signal processing chain detects and flags RFI signals (L3-198) using three strategies, as shown in
Figure 6-13:

- Before channelization, the wideband signal power level is tested for sudden increase on a timescale of a few channelised samples (1.08 µs), compared to the power averaged on a longer timescale (milliseconds). This is indicative of pulsed radio signals (e.g. radar). The flagging threshold, and the averaging time for the shorter and longer timescales are selected by the MCCS.
- After channelization, channels that saturate with respect to the pre-set quantisation range are flagged. The quantisation range is set on a per-channel basis, and saturation is indicative of very high, narrow-band signals.
- The MCCS can provide a per-channel RFI mask for each station. The mask is specified with a coarse time resolution (minutes), based on a priori information (e.g. satellite transit times), or using the results from the calibration and autocorrelation spectra. Packets corresponding to the flagged channels are so marked in the SPEAD header. The CSP may decide how to manage this information.

RFI detection and flagging occurs with a minimum time granularity of one channelised sample. Detection occurs for individual antenna signals, but flagging affects the whole station. The underlying assumption is that an RFI will affect in a similar way all (or most) of the antennas in the station, and that if it is detected in one antenna it is present, below detection, in the remaining ones. Flagginig individual antennas in the beamforming would also cause the beam to be not predictable. Individual antennas can be excluded from the beamforming (and the associated RFI information ignored) before the beginning of an observation scan.

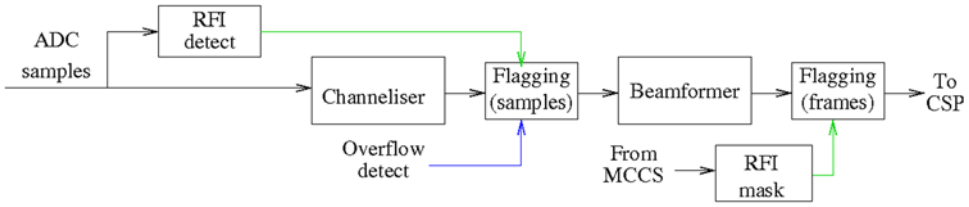


Figure 6-13 RFI detection and flagging in the SPS signal chain

The conceptual block diagram for the wideband RFI detector is shown in Figure 6-14. The ADC samples are squared, to obtain the instantaneous power, and integrated in a short-term accumulator for an integer number *M* of ADC frames (1.08 µs each). Two consecutive integrations are summed together, to smooth the integrator time response. The total integration time is therefore 2*M* x 1.08 µs. The same instantaneous power is also integrated using a single pole low pass Infinite Impulse Response filter, with an integration characteristic time of 2^k samples. This is implemented using a feedback loop with gain $(1-2^{-k})$ and dividing the result by 2^k. Using powers of 2 in the gain allows to implement the filter without using actual multiplications, thus saving FPGA resources and power.

The two averaged powers are compared, and if the short-term accumulator result exceeds that in the long-term accumulator by a programmable factor, the associated frames are assumed to be affected by impulsive RFI.

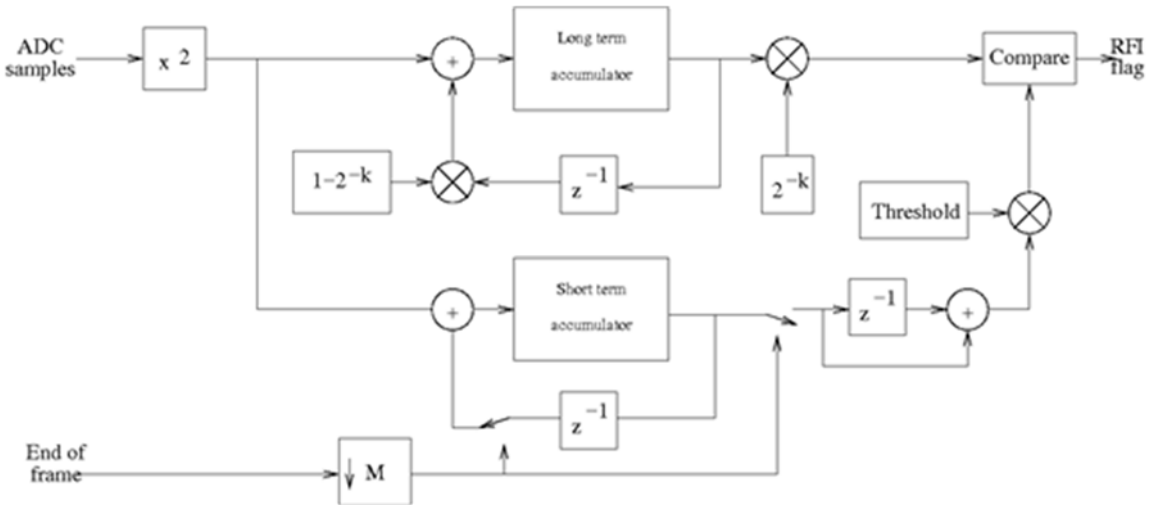


Figure 6-14 Wideband RFI detection block diagram

6.9 Built in Self-Test

Self-test capability is built in each external interface. For functional tests, a test sample generator is present and can produce a known signal, which is substituted to the ADC signal.
LFAA.SPS can run a built-in self-test (BIST) diagnostic while in any off-line or on-line state to detect and isolate failures (L3-117, L3-118, L3-119, L3-122, L3-123 and L3-124). Off-line self-test is only available when LFAA.SPS is in the Maintenance adminMode and causes LFAA.SPS to stop processing data when it is executed. On-line self-test is executed continuously whenever LFAA.SPS is in the Online or Maintenance adminState.
Table 6-4 lists a description of each test that is run and indicates whether it is run during the on-line or off-line self-test.

Test Description	On-line BIST	Off-line BIST
Check DDR4 memory on the ADU processing board to detect stuck bits or other memory faults.	✓	✓
Generate test packets on the MCCS interfaces		✓
Check calculations using “canned” internally generated test vectors and known results at various stages of the processing pipeline inside a TPM.		✓
Check full station beamforming process, using internally generated test vector and receiving the beamformed signal in the MCCS server		✓
Check connectivity on monitor and control networks to verify all devices can be accessed on both networks. This could be as simple as the Cabinet Management periodically “pinging” the Ethernet interfaces on both monitor and control networks.	✓	✓
Check Timecode distribution to ensure both Timecodes are generated and delivered to every ADU board.	✓	✓
Monitor and report optical transceiver transmit/receive power levels as an indication of which end of a communication channel is causing higher than expected BER	✓	✓
Monitor eye diagram on TPM high speed transceivers, using the diagnostic built-in circuitry in the Xilinx FPGA high speed serial transceivers	✓	✓

Test Description	On-line BIST	Off-line BIST
Monitor temperature and fan status of all TPM LRUs and COTS equipment.	✓	✓
Monitor single element power consumption and balance of power consumption across AC mains phases.	✓	✓
Monitor FPGAs on ADU boards for Single Event Upsets (SEUs). Xilinx Ultrascale FPGAs provide built-in facilities for correcting single errors and detecting/reporting multiple errors caused by SEUs (L3-186).	✓	✓
Monitor TPM-ADU internal supply voltages	✓	✓
Monitor all the sub rack power supply voltages, including AC input	✓	✓
Monitor PLL status of the cabinet clock distribution network	✓	✓

Table 6-4 Built-in Self-tests

7 Scenarios

In this section some example scenarios have been chosen to be described in detail. The selection is considered to represent many similar operational scenarios. The following scenarios are documented in the following subsections:

1. A power control scenario that describes how the LFAA.SPS state changes during a staged power up and start up commands.
2. An example of initialisation scenario.
3. An example maintenance scenario that describes how a faulty TPM LRU would be replaced.
4. A possible RFI Detection and Flagging scenario.
5. A scenario for the Transition to Low Power Mode Off-line and uncontrolled shut-down

7.1 Application of Power

Cabinet start up shall be done in two main phases: powering and start up from stand by state.
The powering starts with the manual activation of the main power switch and ends with the STANDY BY cabinet state, with cabinet management board, the auxiliary circuits and the Ethernet switch, required to connect the cabinet to the LFAA management network, active and ready to establish communication with the MCCS servers.

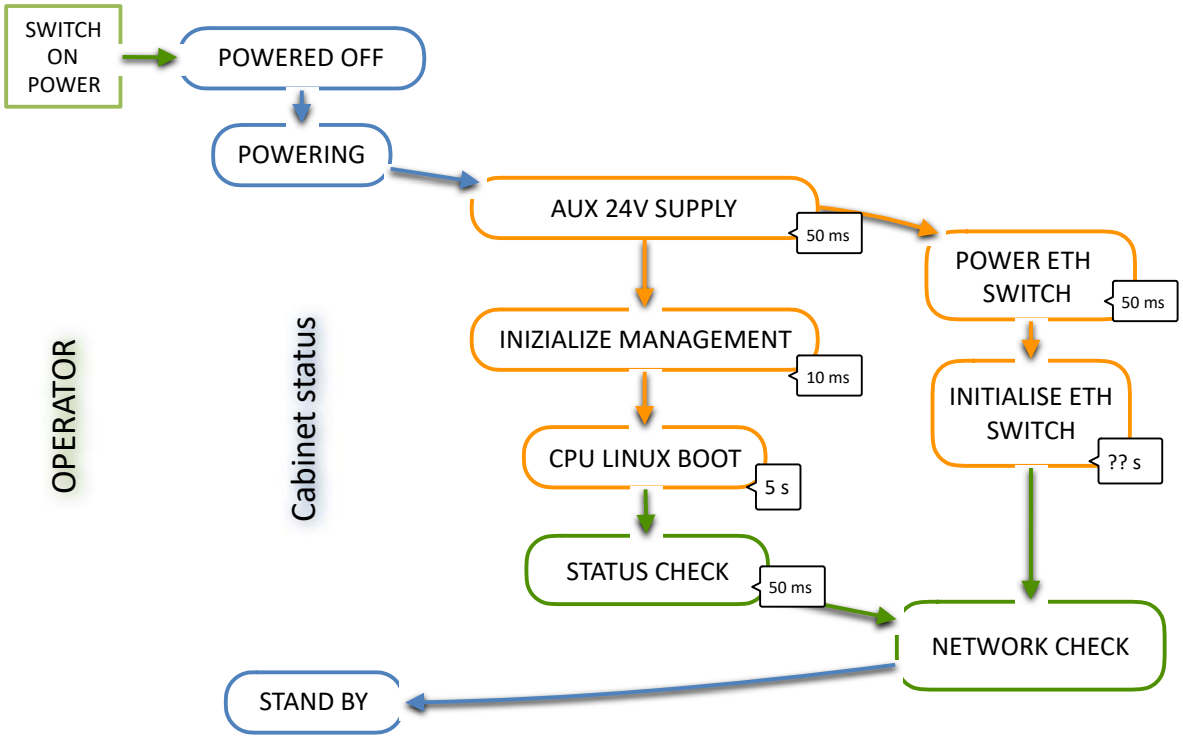


Figure 7-1 Cabinet first power up phase

The time associated to the single steps are summarised in the following table.
The time required to initialise the high-speed Ethernet switch is expected to be greater than 60s and will dominate the cabinet powering phase. It must be noted that the Ethernet switch will be a commercial device and the required start up time can change on a wide range. If a maximum start up time is required, it shall be defined as specification, accordingly with the possible suppliers (Oxford report that the Mellanox 100G switch require more than 5 minutes to operate).

PHASE	STEP	Dependencies	Time worst, s
AUX 24V	1.0	none	0,05
Initialise management	1.1	1.0	0,01
Initialise Eth Switch	1.2	1.0	?? >60
CPU Linux BOOT	1.3	1.1	5,00
Status CHECK	1.4	1,2;1,3	0,05

After the first power up phase it is assumed that the cabinet management board and the network switch are running with the expected and checked status: this condition shall be defined as the "STAND BY" cabinet status. It is assumed that the cooling circuit is not required in this phase due to the low power condition.
The "STAND BY" is the same condition that shall be reached with a command from the MMCS that stops the acquisition of the station bringing the cabinet into a low power condition.
In the STAND BY state the cabinet can accept a START UP command from the MMCS to power up and activate all the cabinet elements to be ready to receive the STATION configuration from the MCCS.
The Cabinet, upon command from the MCCS, moves to a START UP state and begins to supply all the element: the four sub-rack, the other Ethernet switch and the cooling circuit (the sequence shall be defined taking into account the INFRA power distribution requirement).
The time and the dependencies associated to each operation is summarised in the following table:

Operation executed	STEP	Dep	Time worst, ms	TOTAL Time, ms	Item involved
Cabinet second 40G switch powered	1.0	none	1,00E+01		40G second station switch
Cabinet cooling powered	1.1	none			Cooling system
Cabinet management power on the subracks, 220 AC	2.0		4,00E+01	5,00E+01	PDS remote switches
	2.1	2.0	2,00E+03	2,05E+03	sub-rack power supply
	2.2	2.1	3,00E+01	2,08E+03	sub-rack management MCU active
	2.3	2.2	5,00E+03		sub-rack CPU starts boot
	2.4	2.1	5,00E+02		sub-rack ETH SWITCH start up sequence
SUB-RACK MCU POWER ON THE TPMS	2.5	2.2	1,00E+01	2,09E+03	backplane power distribution
	3.0	2.5	3,00E+01	2,12E+03	TPM CPLD and MCU starts to operate
	3.1	3.0	5,00E+01	2,17E+03	TPM management execute the Digital Power ON sequence
	3.2	3.1	5,00E+02	2,67E+03	TPM load the FPGA configuration bitstream, default one
	3.3	3.2	5,00E+00	2,68E+03	TPM management execute a status safety check
SUB-RACK MCU SUB-RACK safety check	4.0	3.3	5,00E+01	2,73E+03	none

Cabinet System monitoring running	4.1	4.0	5,00E+03	7,73E+03	sub-rack CPU OS activated
Request the status to the cabinet management	4.2	4.1			
Sub-rack management board load the configuration to the TPMs and check the system safety	5.0	4.2			

The time requested to execute the LINUX boot is expected to be around 5 second, to be confirmed with the final OS configuration.
The transition state is summarised in Figure 7-2.
The time requested to power-on and activate the sub-rack, ready to be configured by the MCCS is about 7,7 sec, assuming that the TPM firmware is pre-loaded on the TPM nonvolatile memory and the default firmware is loaded.
To complete the configuration of the station from the MCCS only the gigabit management network is required.
To start the acquisition also the second Ethernet high speed switch and the cooling shall be operative.
As before, the Ethernet switch is a commercial device, the startup time can change and it is expected that can be critical.
Few seconds are expected for the cooling system, no critical time is expected.

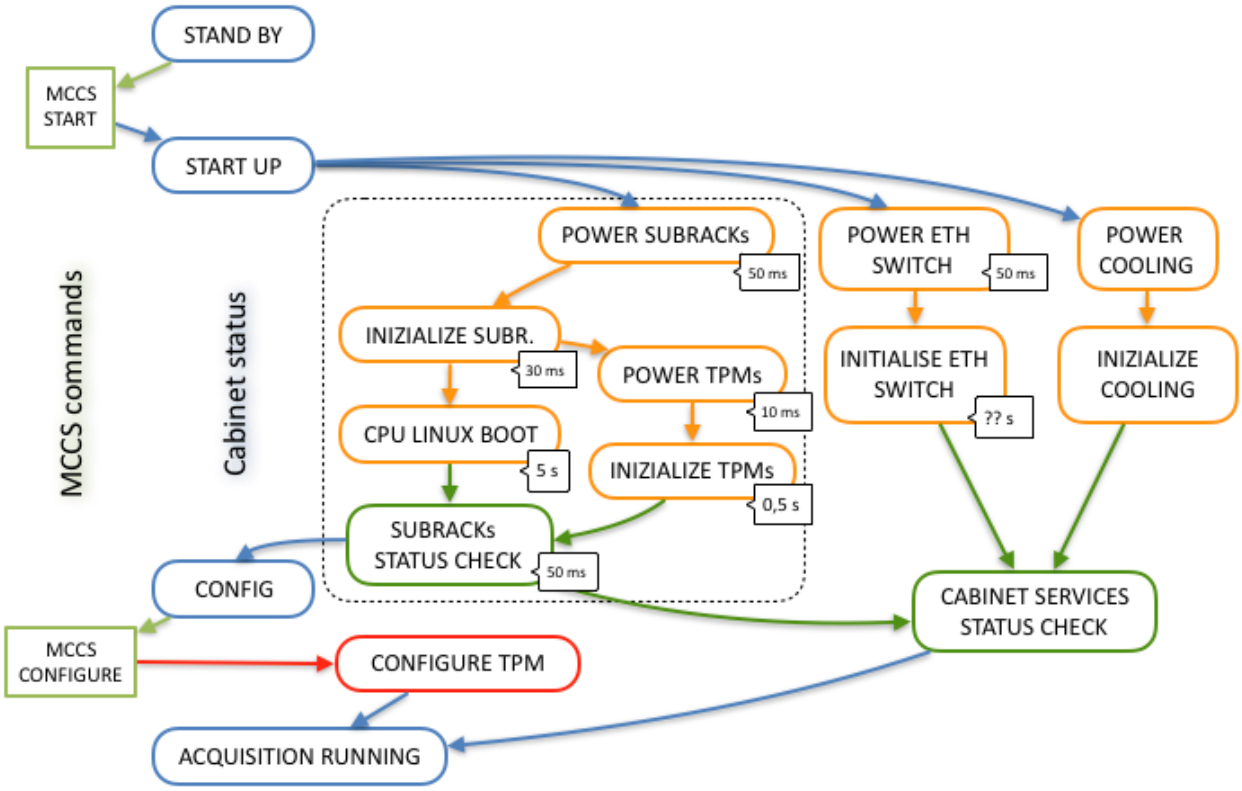


Figure 7-2 Cabinet start up operations

The sub-rack startup executes the following operations:

- power each element in the correct sequence
- load the default configuration on the TPM FPGAs
- activate the board level monitor functions
- verify that all the voltages and currents are in the expected range

- verify that all the components are in the operative status

It is expected that the MCCS after the START command to the cabinet, checks the transition to the CONFIG. Upon that transaction the MCCS can start to configure the TPM with the acquisition parameter and to verify the related status.

7.2 Initialise

When the LFAA.MCCS instructs the LFAA.SPS to transition to the Operational State from Low Power to Ready, the TPMs must be initialised. The sequence is narrated below and depicted in Figure 7-3.

1. MCCS reads the CPLD XML memory map from the TPM. The CPLD memory map is stored in non-volatile memory on TPM and it is accessible after power-up.
2. The FPGAs are programmed. The process can be performed in different way:
    - MCCS directly transfer the bitstream over the network to the TPM and commands the CPLD to write it into the FPGAs configuration memory using SelectMap bus accesses.
    - The same process above can be performed by a Sub-rack or Cabinet Management board, provided that the bitstream file has been previously deployed and written into a local non-volatile memory. In this case MCCS commands the involved Sub-rack or Cabinet Management board to start the FPGA programming process.
    - The CPLD on the TPM programs the FPGAs autonomously reading the bitstream file from local Flash memory. Also, in this case MCCS issues a command to start the process.
3. Once the FPGAs have been programmed, MCCS reads the FPGA XML memory map that is embedded in the running firmware.
4. MCCS issues a command sequence to configure the on-board PLL to generate required clocks. Presence of 10 MHz Reference clock is checked.
5. MCCS issues a sequence of commands to program the ADCs. At the end of this phase the ADCs are waiting for the FPGAs to establish the JESD204B links.
6. JESD204B initialisation is commanded and supervised by MCCS accessing the control and status registers of the JESD204B core in the FPGAs. After successful initialisation, data are being transmitted by the ADCs on the JESD204B lanes and the FPGAs are correctly receiving the data.
7. MCCS commands the TPM to start initialisation of the following devices:
    - DDR memory
    - FPGA to FPGA data link
    - 40G Interface

    Once commanded the FPGA performs the initialisations autonomously. MCCS can check related status registers to verify whether the initialisation has been successfully executed. In case of DDR and F2F link the initialisation, procedure includes the execution of BIST. 40G initialisation requires that a valid link is established between the TPM and the 40G switch port; link presence is checked at the TPM and at the switch side to guarantee that each TPM can receive and transmit data.
8. MCCS programs UTC time into FPGA and check for synchronization of the time counter in the FPGAs. Subsequently, MCCS verifies that the FPGAs sample correctly the PPS and applies compensation delays on the incoming data in the digital domain if necessary. Time and PPS synchronisation requires that the FPGAs receive at two PPS rising edge.
9. MCCS programs the DSP pipeline transferring the required parameters to the TPMs such as calibration coefficients, pointing delays and delay rates, re-quantisation factors, etc.
10. When the TPM transitions to READY, it waits for a command from MCCS to start data forwarding to the DSP pipeline.

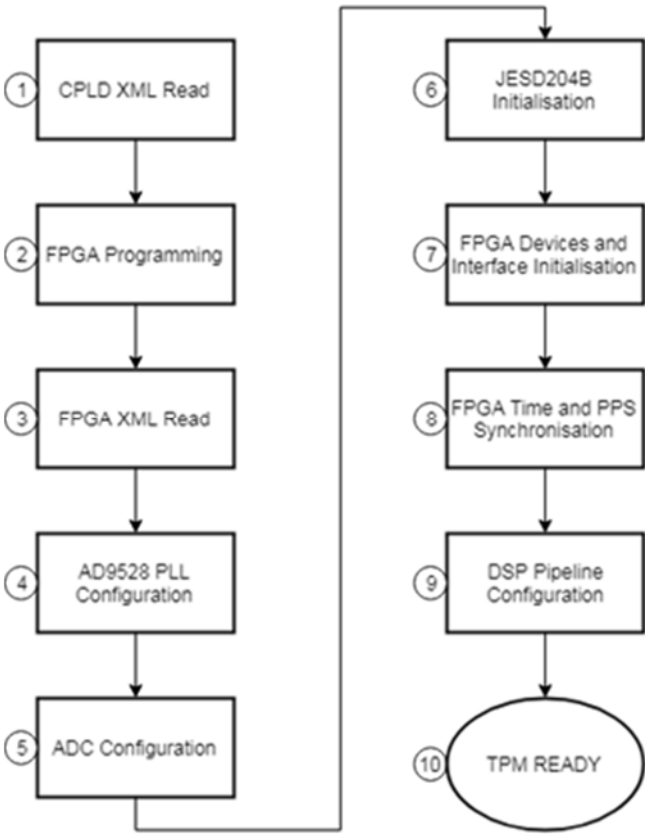


Figure 7-3 Initialisation Sequence Diagram

7.3 TPM LRU Management

This section describes an example maintenance scenario involving faulty TPM LRU hardware. The sequence of events starts with SKA Operations receiving an alarm or drilling down to find a TPM LRU with a Tango device state of FAULT or ALARM. Engineering operations is expected to set the administrative mode of the LRU to MAINTENANCE to identify it as being unable to be used within a sub-array for normal data processing.
Diagnostics can be executed on the TPM LRU and an engineer is expected to check the test mode info results and make a decision as to whether the fault is due to software, FPGA code or hardware. It may also be useful to examine the event log for the LRU. The process of replacing TPM LRU hardware, which is physically a LRU that inserts into a sub-rack, is described in the following procedure. This starts with a maintainer on site with a replacement TPM LRU:

1. The faulty TPM LRU is identified from rack, sub-rack and LRU location labelling provided by the MCCS Hardware Configuration Database
2. The TPM LRU is powered down
3. The maintainer should wait until the power indicator LEDs on on the subrack-management, related to the TPM LRU are off.
4. The TPM LRU cables are removed and capped, keeping a note of their locations.
5. The TPM LRU is extracted from the sub-rack
6. The replacement TPM LRU is inserted into the sub-rack.
7. Once the LRU is fully inserted it will enter a low power standby mode.
8. Cables are reconnected into their original positions.

After LRU replacement, the LRU Tango device state should be STANDBY. The maintainer should change the operational state of the LRU to INIT. Self-tests are executed automatically during bring up. LRUs that fail these self-tests show a Tango operational state of FAULT, instead of ON, after bring up. Fault resolution only completes when the Tango LRU state ends in ON. The LRU will be ready for operations when the maintainer sets its admin mode to ONLINE.

7.4 RFI Detection and Flagging

RFI detection and flagging (L3-198) occurs automatically, as described in section 6.8, and involves the RFI detector, channeliser and beamformer in the TPM firmware. MCCS participates to RFI mitigation by setting up these elements, monitoring their status and reporting to TPM any RFI event.
As a possible use case we will consider the RFI emission from an approaching aircraft plane, involving packetised radio transmission in a relatively narrow channel (e.g. transponder). In the end the RFI power will be strong enough to saturate the ADC.
When the aircraft is very far (hundreds of Km), the emission is well below the sky signal received form a single antenna. It is however sufficiently strong to saturate the affected channel, after channelization. As the aircraft approaches, it increases the received signal level during packet transmission. The RFI detector then flags the corresponding time intervals for all channels. MCCS notices the increase in RFI flagging activity and notifies TM. At some point, when the aircraft is close to the station, and the received signal power increases by more than an order of magnitude, the measured power level exceeds the static power threshold and all samples sent to CSP are flagged.

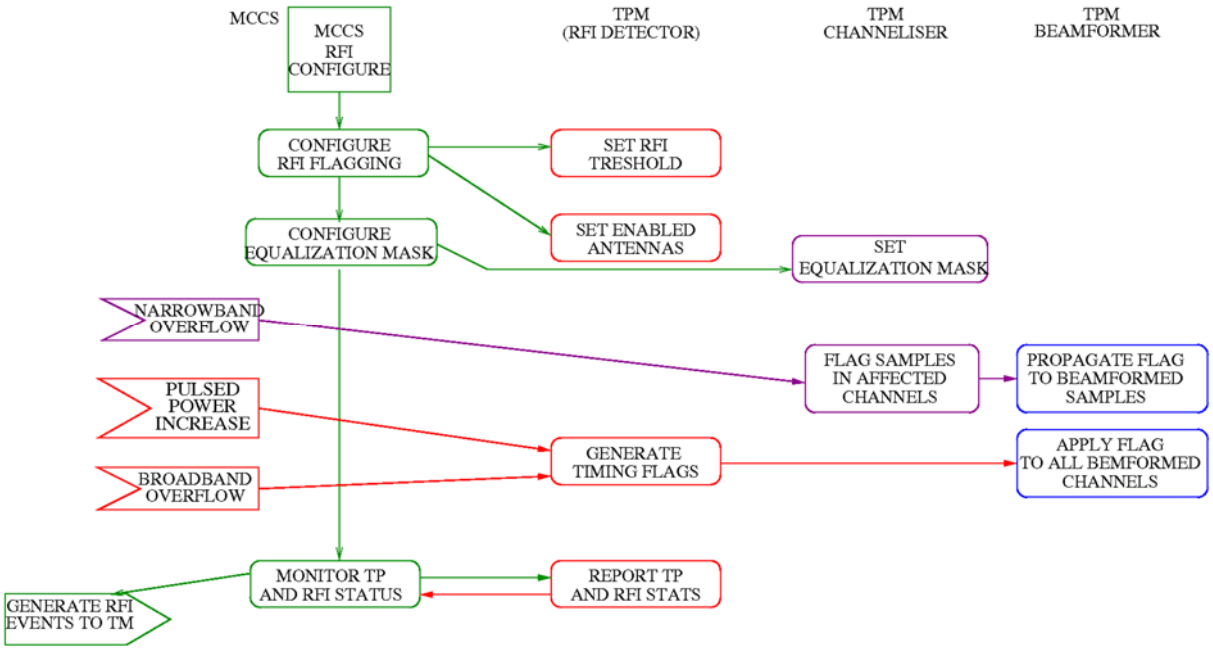


Figure 7-4 - RFI Detection and Flagging Use case

The corresponding activity diagram is shown in Figure 7-4. MCCS configures the RFI detector and, based on the expected power level, the number of bits to be discarded in each spectral channel (equalization mask). RFI from the incoming aircraft generates, in succession, the “Narrowband overflow” event (in the channeliser), the “Pulsed Power Increase” and the “Broadband overflow” events (in the RFI detector). The channeliser reacts to the first event by flagging the affected channel(s). The RFI detector transmits the flagging information to the channeliser, which in turn flags all channels for the affected time interval. The beamformer propagates the flagging information to the beamformed samples.

In the meantime, MCCS monitors the RFI detector and reports the RFI statistics to TM.
TM can specify an RFI mask in advance e.g. to mask off channels known to be affected by the incoming aircraft. As this feature is also present in the CSP, with much better frequency resolution, it is probably not worth being used in the LFAA.

7.5 SPS Failures

SPS can suffer failures at any point, including during power up or in low power mode, during initialization and operation. For hardware failures, the hardware is switched off, its status is changed to FAULTY and TM is notified. MCCS has a hardware configuration database which, apart from storing the configuration of all hardware components, contains their hardware locations within the CPF and RPF to aid maintenance personnel to quickly localise the equipment.
The largest SPS unit is the cabinet. Groups of devices within a cabinet can become unreachable or unusable depending on which hardware device(s) fail. The worst-case scenario is when a CMB fails, since it is responsible for the distribution of signals and network to all SMBs in the cabinet. The resulting effect is that the entire cabinet (two stations) become unusable. The same effect occurs if the AC power distribution fails (and the cooling system, however in this case it would be possible to perform a proper shutdown of the equipment)
Each SPS cabinet contains two 100Gb switches which connect the cabinets with each other as well as with MCCS. If one of the switches fails, then the TPMs connected to it cannot be part of a station since they will be unable to transmit the partial beamformed signals. There is enough redundancy between cabinets such that LMC communication with MCCS can still be routed. If both two switches fail, then the cabinet will be totally unreachable.
TPM failure and replacement is described in Section 7.3.
For all devices failures the same procedure is employed, as described for the TPM LRU in Section 7.3. The steps required to physically replace the hardware component will change, however one the new LRU is attached then automated software (both in the device itself and in MCCS) will take over and perform diagnostic checks. When all the tests pass, and the component is fully initialised then it is placed in the ON state (and admin mode to ONLINE).

7.6 Transition to Low Power Mode Off-line

Cabinet shall be powered down in two steps: stand by and then completely unplugged.
In the first step a MCCS command stop the STATION sub-racks, one network switch and the cooling system. The cabinet comes back in the STAND BY state still able to turn on to the normal acquisition modes.
The transition diagram is the following:

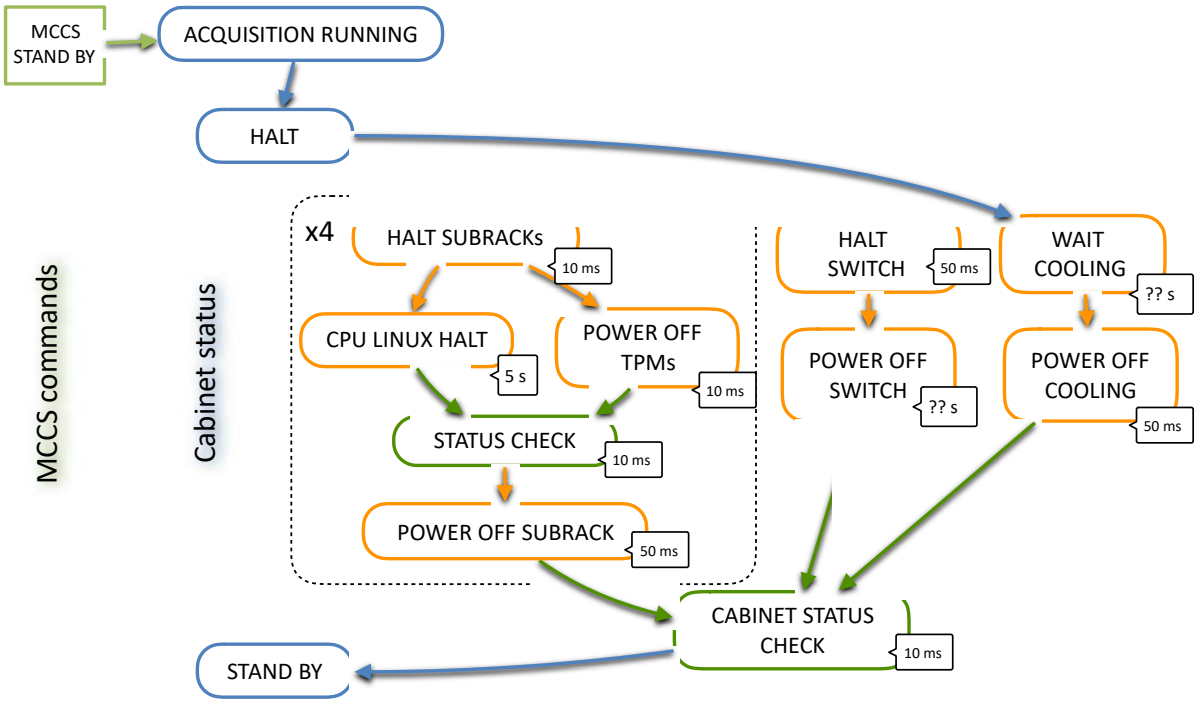


Figure 7-5 Cabinet stand by procedure

The time required to power-off the Ethernet switch is undefined and again can be different for each product. The cooling shall wait some time to extract the residual heat from the system before the final shut-down. The requested timing shall be investigated further, several seconds can be required to maintain thermal specifications.

To complete the shut-down process and unplug the cabinet from the INFRA power distribution network, the steps described in the Figure 7-6 shall be executed.

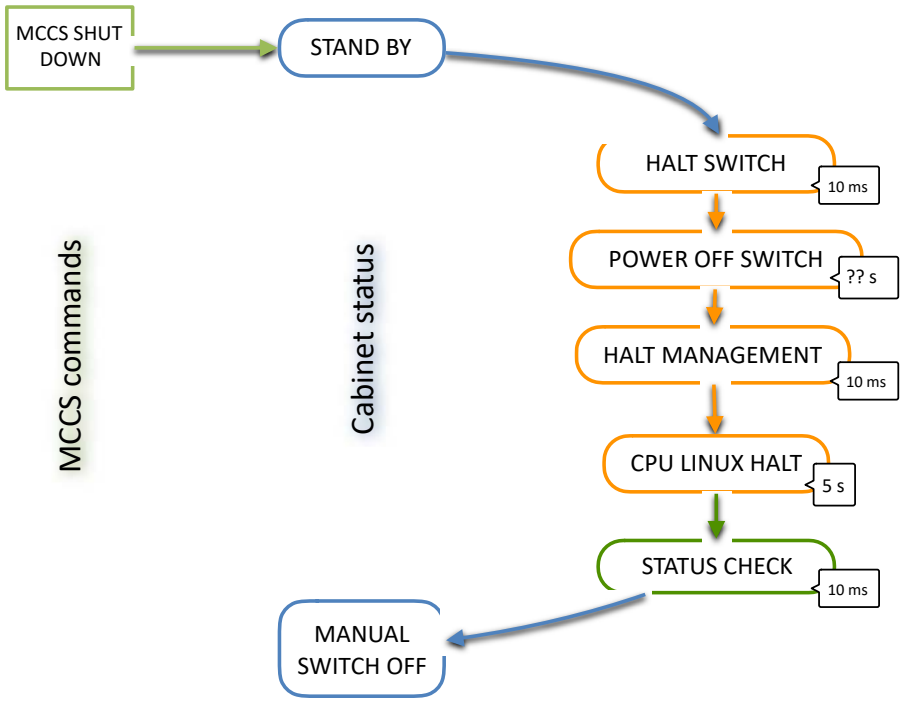


Figure 7-6 Cabinet off line procedure

The MCCS shall send the SHUT DOWN command to the cabinet to start the procedure. The management board shall send the HALT command to the network switch and then power-off the switch when his procedure is ended.
After that the management shall execute the halt procedure of the OS and a status led on the front panel shall signal to the operator the flag to switch off the main supply.

7.7 Uncontrolled Shutdown

With the current cabinet design, if the techniques proposed to manage the supply transient has been implemented (9.5.3), the unexpected shutdown should generate the following effects:

- improper shutdown of the stations subracks, with exception of the sub-rack management board,
- improper shutdown of the network switches,
- shutdown of the cooling system,
- shutdown of the cabinet auxiliary supply,
- managed shutdown of the cabinet management board and the subrack management board.

The proposed battery feature for the management board provide the capability to execute a complete Linux OS halt procedure before that the management supply is missing avoiding possible file system corruption and data loss and reducing also the subsequent boot up time.
The undesired effect of the improper shutdown is expected mainly on the Ethernet high speed switches. These commercial devices are internally structured with a complex CPU and a proprietary Operative System that can require a controlled shut-down procedure. An improper power lack on these components can cause OS file system corruption with several possible effect, from negligible to severe, depending to the switch type.
On the cooling circuit, the improper shutdown halts the liquid and airflow circulation; it is expected that in some points the temperature rises. No relevant effects are expected but this behaviour shall be verified in the cabinet testing.
No effect is expected on the TPM with exception of data corruption if unexpected shutdown will occur during a non-volatile write operation (i.e. FW update). In this case the process shall be re-started with a recovery procedure without manual operation on the board thanks to the dual boot feature. A default factory firmware is loaded if a corrupted configuration file is present in the user non-volatile memory.

8 Design Decisions

In the table below are reported all the design decision carried on for the development of SPS equipment from the prototype to the current LFAA version.

Cabinet Level				
Design Decision	**Related risk**	**Risk level**	**Expected effect**	**Mitigation**
Cabinet design based on subrack assemblies	Higher cost and complexity	Low	Run out the budget	Prototype and verify production costs
stations	High integration	Medium/low	Difficult board handling	Accurate design for maintenance
Distributed AC-DC power supply	supplies module involved	Low	Changing supplier	Find multiple power supply sources
Easy installation/maintenance of installed boards	Higher design costs	Medium/low	backplane board	Prototype and verify production costs
separation	Higher design costs	Medium/low	Run out the budget	Prototype and verify production costs
modulation inside clock	verified. EMC at cabinet level and possible	Medium/low	Analogue acquisition performance degradations	EMC levels
cables	signal	Medium	spectra	Use fibre optic
(32) ports 40G commercial ethernet switches	High cost	Low	Run out the budget	among TPMs in the same sub-rack
No UPS at cabinet level	Uncontrolled shutdown, longer recovery time	Low	unpredicted supply loss	Accurate elements design and test
CPF	connection	Low	that is negligable	Going back to splice cabinet solution
Sub-rack Level				
Design Decision	**Related risk**	**Risk level**	**Expected effect**	**Mitigation**
Eight (8) TPMs per sub-rack	Power density increase	Medium	Temperature increase inside a sub-rack	High efficiency cooling system
distribution	Design complexity increase, poor connectors	Low	Malfunctions, performance loss	Accurate design and test
TPM cooling system by heat pipe techonology	Higher design costs	Low	Run out the budget	Prototype and verify production costs
Backplane design integrated with cold plate design	interface	Medium/low	Poor thermal transfer, mechanical contacts	Prototype & verify sub-rack integration
Clock distribution on the backplane	Possible interference with digital signals	Medium/low	Interference noise on the 10 MHz ref clock	clock quality
TPM Level				
Design Decision	**Related risk**	**Risk level**	**Expected effect**	**Mitigation**
technologies	40G electrical signals	Low	Increased signal loss	Shielding and accurate cable routing
ADU and pre-ADU separate PCBs	Higher cost	Low	none	respective internal layers
Remove uController from version 1.2	Cabinet management	Low	levels	procedures
Two (2) FPGAs per ADU	Syncronization and data sharing between FPGAs	Low	Higher firmware complexity	and verification
Eight (8) bit output equivalent connection for each ADC	More than eight (8) bit resolution needed	Medium/low	Inadequate RF performance	Detailed signal model analysis
Standard 6U mechanical format	Signal interferences	Medium	Reduced analogue performance	Accurate layout and test
ADC converters by Analog Devices	Single source components	Medium	Possible components unavailability	Agreement with Analog Device supplier

Table 8-1 Design decision

9 Performance

To acquire and process all signals from the Field node, a special SPS cabinet will be provided for the central core and for the outer stations. The mentioned cabinet system for both locations will contain the acquisition electronics and the related functions, required for the LFAA.
The main requirements to drive the cabinet design are:

- TPM boards are the basic element, receiving 32 signals each with 16 WDM receivers, standard 6U rack mount size.
- 256 single side cabinets containing 32 TPMs each (8200 TPM total)
- Clock distribution network from a single source to each cabinet with a 10 MHz and 1 PPS signals
- Control/data network based on 40G and 10G optical/copper (QSFP+) cabinet level links
- Three-phase 360V AC power supply
- 8°C water for liquid cooling to each cabinet

It considers also non-functional requirements like:

- Whole-of-Life Cost
- Energy Efficiency
- Capital Cost
- Reliability
- Maintenance

Thus, the performance of SPS Cabinet system derives as result of the design criteria mentioned before. Details are provided in [RD12].

9.1 Signal Quality

9.1.1 General

Below there are reported tables summarizing the functional specifications of the receiving chains including ADC. These numbers have been used as acceptance level for the AAVS1 prototype and therefore is still valid the assumptions that these specifications consider as a receptors SKALA2 antennas + differential LNA and a compatible RFI panorama as reported to the monitoring campaign carried out in 2013 [RD67].

DC specifications (at 25°C unless otherwise noted).

Parameter	Value	Notes / Conditions
Vin FE PCA	3.5-5VDC	
Power FE PCA	<750mW	At 70°C with Vin=3.5V and without the LNA boards connected and biased.
Vin PREADU PCA	3.5VDC	
Power PREADU PCA	<1300mW	Two PREADU channels.
LNA Power Supply	3.5-5VDC >150mA	The FE module shall bias the LNA through the RF connectors.

Optical specifications.

Parameter	Value	Notes / Conditions
Nominal WDM optical wavelengths	1270nm / 1330nm	

RF requirement specifications (0-10Km of G652D SMF).

Parameter	Value	Notes
RF band	50-350MHz	Overall frequency band
Flatness	+/-1.5dB	
HP filter rejection	≥50dB	Freq≤20MHz, HP filter integrated in the FE PCA
LB filter rejection	≥50dB	Freq≥450MHz, LB filter integrated in the PREADU PCA
Gain	41dB	See Simulation report.
IRL	>12dB	
ORL	>12dB	
NF	<22dB	
RF channels isolation	>30dB	Defined as the difference of the gains measured at the two PREADU PCA outputs with the same FE PCA input.
OP1dB	>+17.3dBm	20dB below P1dB at nominal output power of -2.7dBm.
OIP3	>+18dBm	See Simulation report.
OIP2	>+38dBm	Updated spec considering RFI statistic.

Environmental specifications.

Parameter	Value	Notes
FE PCA operational temperature	-10 ÷ +70°C	
PREADU PCA	+15 ÷ +30°C	

Table 9-1 RX specifications from the output of LNA to input ADC

Sampling frequency: 800 M SPS---Bandwidth 50 – 355 MHz	
ADU Performance Parameters	
Signal to Noise Ratio referenced to Full Scale [dBFS]	> 48.6
Gain Flatness [dBFS]	< + 0.5
2nd – order Harmonic Distortion [dBc	< -66
3rd – order Harmonic Distortion [dBc]	< -62.5
Worst Other Spur [dBC]	< -60
Spurious Free Dynamic Range [dBc]	> 60
ENOB [bits]	> 7.8
Cross-Talk [dBc]	< -47

Table 9-2 ADC specifications

9.1.2 Beamforming

Beamforming is performed on each coarse channel, by adding a phase factor to each antenna signal, and summing the signals from all antennas in a station. Phase is computed by linearly interpolating the expected geometric delay, multiplying the delay by the channel nominal frequency, and computing the phasor using a lookup table. Possible phase error sources, translating in a decorrelation of the resulting beamformed signal, are:

- Finite phase resolution of the phase lookup table
- Finite accuracy of the phase calculation
- Difference between the actual phase as a function of the frequency, and the constant phase across the channel width.

The first term also creates a sawtooth phase modulation, with amplitude equal to the lookup table phase step, and frequency proportional to the delay rate. For a beam tracking at sidereal delay rate, at the maximum frequency (350 MHz) and antenna distance (20 m), the phase step frequency is of the order of 1-2 Hz. This modulation may create artefacts (sidelobes) of strong spectral lines, but spectral regions affected by strong RFI lines will be unusable anyway and this effect is negligible.

9.2 Latency Performance

9.2.1 Reconfiguration Time for Processing Resources

Reconfiguration of processing resource is performed by executing the initialisation procedure depicted in section 7.2**Error! Reference source not found.**; the critical and most time-consuming steps in the process are bitstream configuration and establishment of 40G links.

When FPGA configuration is directly managed by MCCS transferring the bitstream file to the TPM, a certain amount of time is needed for transmission over the network. When MCCS needs to program several TPMs, the programming time depends mainly on the MCCS capability to execute the procedure concurrently. However, this can be mitigated by using broadcast communication to distribute the bitstream to the TPMs; this has been evaluated in the prototype and resulted in programming time of a station in the order of 2 seconds. Furthermore, FPGA programming can be offloaded to Sub-Rack or Cabinet Management Boards and hence executed locally and concurrently. As last option, the FPGA programming can be performed autonomously by the TPM after receiving a command from MMCS. In this case the expected programming time is less than 1 second.

The establishment of 40G link between a TPM and related switch port requires that:

- The FPGA has been programmed, Ethernet Reference Clock is running and 40G core has been reset.
- The switch has booted up and it is ready to accept a connection. The boot time depends on the specific switch model and, provided that the switch is ready, the process of link establishment still requires a certain amount of time which depends on the specific switch model. In case of Mellanox SX1012 switch used in the prototype, boot time can be evaluated in about 4 minutes, while link establishment requires about 9 seconds.

In reference to the initialisation sequence depicted in 7.2 and noting the points above, a reconfiguration time of less than 24 seconds, as required by L3-188, can be achieved considering that only a subset of the initialisation steps have to be executed sequentially.

Specifically, steps 1 to 6 of Figure 7-3 are required to be executed sequentially, while step 7 to 9 can be executed in parallel. The first 6 steps can be executed in about 6 seconds; the remaining time to finish the initialisation is then mainly constrained by 40G link establishment time, which adds additional 10 seconds. Overall a reconfiguration time of 16 seconds should be achievable.

It should be noted that it is not possible to meet L3-188 when the reconfiguration time includes the100G switches boot time.

9.2.2 Alarm Responding

Alarms generated by SPS need to be propagated to MCCS, which in turn notifies TM (and other parties) of this such that appropriate action can be taken. The latency between a sensor readout and notification to TM is the accumulation of the following times:

- The sensor polling times. This should be set depending on the change rate of the sensor itself. For example, if temperature values are assumed to change with a rate of 1 degree per second, then a minimal polling period of 1 second should suffice. A high polling period result in higher network traffic and processing requirements, whilst a low polling period can result in a high latency for detecting a value which is beyond an alarm threshold.
- A read request must travel across the SPS and MCCS networks, be processed by the LRU, and the request travel back across the SPS and MCCS networks. The number of hops through which these packets go through depends on the physical location of the LRU, however it should be anywhere between 4 and 8 hops. The latency induced here should is less than 1ms
- Once the read value reaches MCCS it is handled by the TANGO LMC infrastructure. The latencies are therefore defined by TANGO, which typically in the order of tens of ms. This depends on how deep the TANGO hierarchy is (through how many devices the alarm must go through) and the load on the system. MCCS should be capable of raising an alarm within 100ms of reading a sensor value

The sum of the above latencies should result in a total latency of less than 600ms, as required by L3-187.

9.2.3 Beamformer Latency

Samples are labelled in the ADC interface. Absolute sample time stamping is therefore independent from latency in other SPS elements. Samples are however available at the CSP after a large latency, with possible latency scatter among different stations.

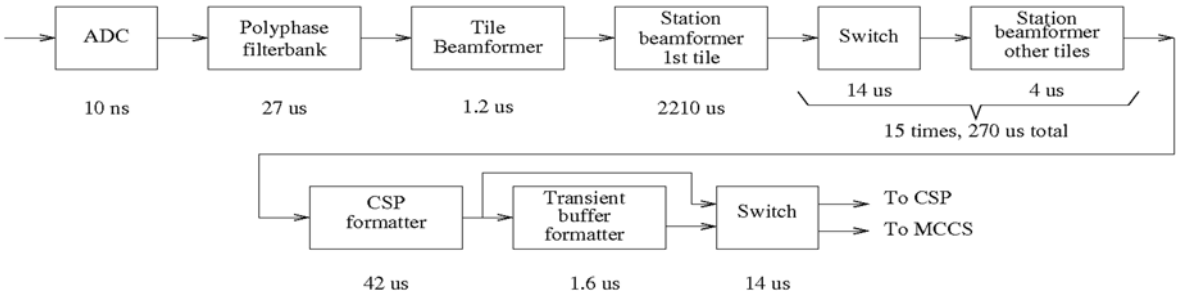


Figure 9-1 Latencies in the signal processing chain

Latency introduced by different elements is summarised in Figure 9-1. The largest part of the latency is due to the necessity of accumulating 2048 channelised samples for one CSP sample frame. This is performed in the station beamformer, and is shown for the first tile only, as this latency is simultaneous in all tiles and does not add up.

Polyphase filterbank introduces a latency mainly due to the necessity of filling the FIR filter. This requires about 25 µs, while other 2 µs are required by the FFT engine. Tile beamformer adds another 1.2 µs in the channel selection process.

The latency due to the UDP-IP formatter, transmitter, receiver and Ethernet switch has been measured in the range of 12 to 15 µs, with an average of 14 µs. Optimization of the buffering schemes

may reduce this slightly. The processing time for the beamforming packet is about 4 µs. These times must be multiplied by 15, i.e. the number of hops in the beamforming process, for a total of 270 µs.
The CSP formatter must wait for 8 beamforming packets to build one CSP packet. This requires 42 µs. Final UDP-IP processing and the 40 GB switch add other 14 us.
In the end, CSP will begin to receive beamformed packets after 2564 µs from the nominal start of the integration. Packets arrive in sequence for different frequency channels/beams/substations, with each packet carrying samples for 2.1 ms and the packet for the last channel arriving with a further latency of about 2.1 ms (4.6 ms total) (L3-226). This latency is mostly deterministic, but some scatter is expected. Scatter is mainly due to the scatter in the network times and is of the order of ±20 µs peak, and 3-4 µs RMS after 16 hops. Each station sends packets to CSP with an average spacing of 5.76 µs, so arrival order of packets from different stations could not be guaranteed.

9.2.4 Transient Buffer Latency

Transient buffer packets are formatted and sent to the transient buffer in MCCS just after the corresponding packet has been sent to CSP. This process requires about 1.6 µs in addition to the beamforming total latency of ≈2.6 µs.

9.3 Power Consumption

In the table below are summarised the power consumption of the main devices installed on ADU board and the power requested by the analogue circuitries from the pre-ADU.
The main gain in terms of power saving between R 1.2 and R 1.5 depends on the new ICs used to populate the board respect to the AAVS1 version, an optimization of the FPGA code or the simplification of RF circuitries as the pre-ADU case. As mentioned in several part of this document, fine tuning of the performances of the TPM boards (preaADU and ADU) and, in particular, FPGA FW, are still in progress so our expectation in the future generations, is to improve these characteristics respect today with the target of 100W each one.
The power consumption of the current design of preADU is as reported below:

preADU	0023E (mA)	0015E (mA)	0015E (mA)	1017E (mA)	Itot_RF (mA)	I_dig (mA)	Vdd (V)	Pch (mW)	Prx_WDM (mW)	P_preADU (W)	P_TPM (W)
T = 25°C	34	36	36	66	172	8	3.5	630.0	1260.0	20.2	20.2
T = 40°C	36	37	37	67	177	8	3.5	647.5	1295.0	20.7	20.7

Table 9-3 Summary of the power consumption of RF and digital devices installed on board

In the next release of the ADU board we will consider the possibility to insert VGA differential amplifiers as ADC driver, so the power consumption of the preADU can be decreased to only about 7.8W (10.6W) because we can remove the last two (one) stage of amplification and all the digital electronic for controlling it (the VGA is directly controlled by ADU) from the current design. From the component specification, gain capability, both the last two stage of amplification can be removed but because the antenna design is still open, the second option is maintained as worst case.

Peripheral \ Board Release	R 1.2	R 1.5 Worst Case	R 1.5 Typical	R 1.5 Cost option
Digital IC				
CPLD, Eth, Flash	3	2	2	2
CPU	0.5	0	0	0
FPGA x 2	55	52.0	46.2 (*2)	40
DDR memories	3.4	5	2.7 (*3)	2.7 (*3)
Analogue (800 MHz)				
PLL, CLK Buff, 10G PII	3.6	3.6	3.6	1.6
ADC	52.6	25.1	25.1	25.1
VGA		7.128	7.1	7.1
Front End	16.7	10.6	7.06	7.06
Power distribution efficiency:				
Digital:	90.25%			
Analogue (150mV linear drop):	82.1%			
Total Digital IC Watts:	68.6	65.4	56.4	52.1
Total Analogue IC Watts:	68.4	43.6	43.6	41.2
Front End	18.5	11.7	7.8	7.8
TOTAL Supply, Watts:	**155.5**	**120.7**	**107.8**	**98.5**

Table 9-4 Summary of the power consumption per TPM

(*1) The large memory array changes from a 2 GB DDR3L to a larger 16 GB DDR4, running at the same speed.
(*2) FPGA power consumption updated with the new Xilinx power estimation spread sheet, released on June 2018.
(*3) Power estimation has been updated for different size and bank organization, 4Gbit x8 x2, total capacity 8 GB due to the removed transient buffer requirement.

9.3.1 Power Consumption During Function Mode Change

The cabinet and the related element design allow a controlled and incremental the startup sequence and multi-level monitoring capabilities.
A possible startup sequence is reported in the following table:

Step	Supply	Element supplied	Available functions	Requested power	Power %
0	None	None	None	0	0%
1	Aux AC-DC 24V	Management & AC PDS	Cabinet management	125	3%
2	40G Switch 1	40G Switch 1	Network connection to LFAA	325	7%
3	Cooling AC-DC 24V	Cabinet cooling	Cooling available	759	15%

4	Subrack 1,2	Subrack 1,2 management	Station 1 management	813	17%
4.1		Station 1 TPM	TPM management	1293	26%
4.2			TPM ready to run	1613	33%
4.3			Station 1 running	2735,8	56%
5	40G Switch 2	40G Switch 2	Network connection to LFAA	2935,8	60%
6	Subrack 3,4	Subrack 3,4 management	Station 2 management	2989,8	61%
6.1		Station 2 TPM	TPM management	3469,8	71%
6.2			TPM ready to run	3789,8	77%
6.3			Station 2 running	4912,6	100%

The cabinet shall be powered-on manually by a dedicated input switch. At the power-on only the auxiliary 24V supply is active and the cabinet management board starts to operate.
The management board can be pre-programmed or remote-controlled to manage all the startup sequence. In the cabinet the management board will control the power supply switches and will configure and run the other boards by ethernet based commands.
As a first step, if requested, the management can power-on the first 40G switch supply to provide the connectivity with the LFAA network.
After that the cooling circuit shall be started; the requested power in the first steps can be lower due to the cabinet partial power activation.
Then the TPM sub-racks can be powered to start the station power-up sequence; a single sub-rack or all the four sub-racks can be activated together for a different power up scheme.
Powering a sub-rack, only the backplane and the sub-rack management board are powered and starts to operate in few seconds. The network function is available, and the sub-rack management can receive the ethernet base commands to proceed with the startup or can be programmed for automatic startup.
Each sub-rack TPM can be powered and verified for the absorbed current. When powered-on the TPM provides only the management function, ready to be programmed. Also, the TPM internal power distribution is partially OFF. It is possible to power in the digital section and the analogue section separately; by default, at power-on only the management section of the TPM is powered with a small power consumption.
At this point the management board can power-on the requested TPM section and can program the FPGAs, set the working frequencies in the PLL, supply and configure the ADC and the optical receiver circuit. In these steps, the absorbed current can be monitored at backplane level and verified against preset values and in case of variations, an automatic shut-down can be programmed. If everything is fine, the TPM is ready to run. In the last step the ADC and the VGA can be placed in the sampling mode to start the acquisition.
In the proposed cabinet power-on sequence, the two station are powered on separately, just to detail the system capability. It is possible to power-on the stations together with a different power sequence.

9.4 Thermal Performance

The SUB-RACK's units include 8 boards, 1 power supply unit and 1 Management Board, with a power of 800 W equally distributed on each board:

- PTPM ≈ 100 W for each Board

- PSUB-RACK ≈ 800 W for each SUB-RACK

The SUB-RACK will be connected externally to a liquid circuit to remove the heat from inside. For doing that, we will use an Heatpipe System directly in contact with the electrical components on the boards to transfer the heat to the opposite side of the board where is placed a Liquid Cold Plate (LCP) connected to the external liquid circuit

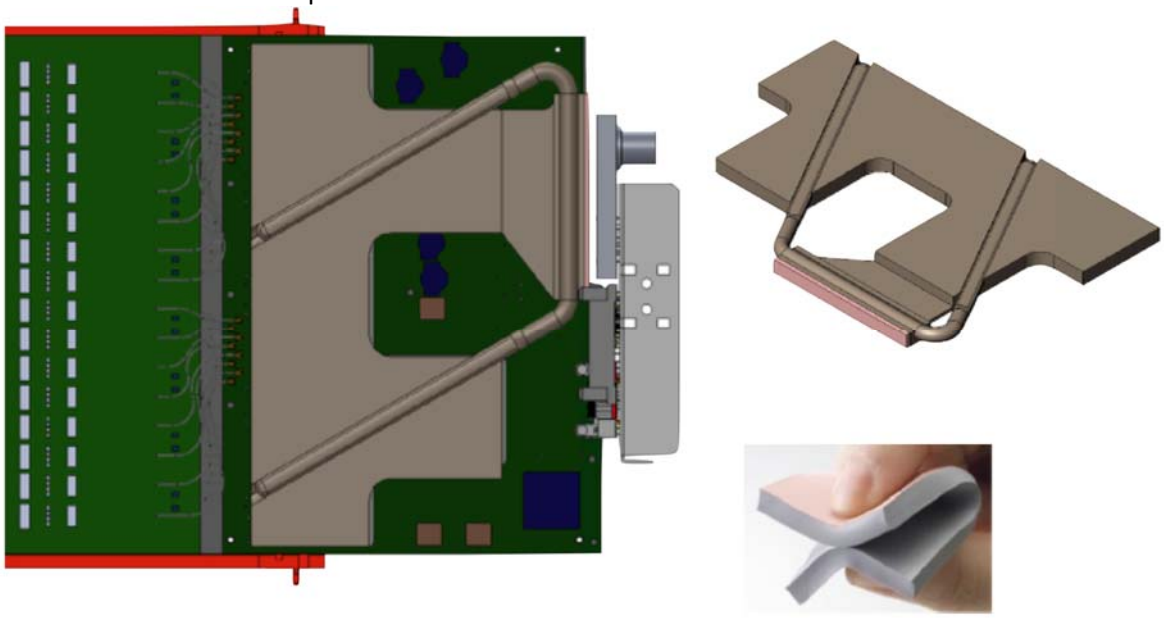


Figure 9-2 Heatpipe and its installation on TPM, on the right bottom the soft thermal pad

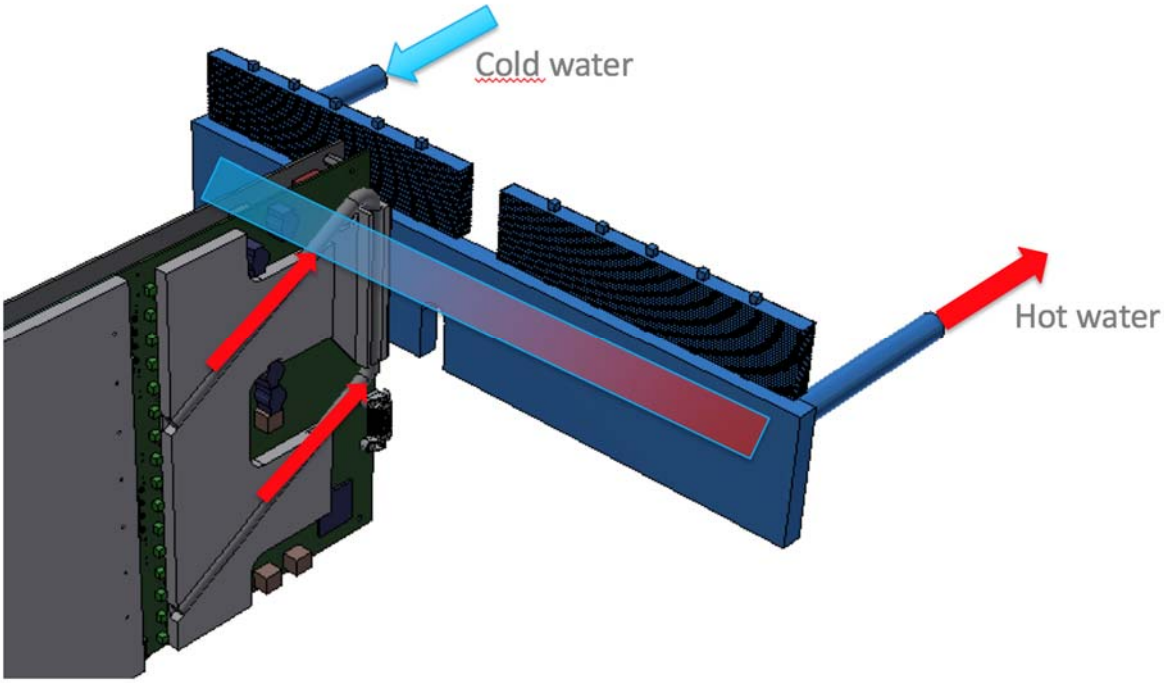


Figure 9-3 Mechanism of the heat transfer from heatpipe to the coldplate and liquid

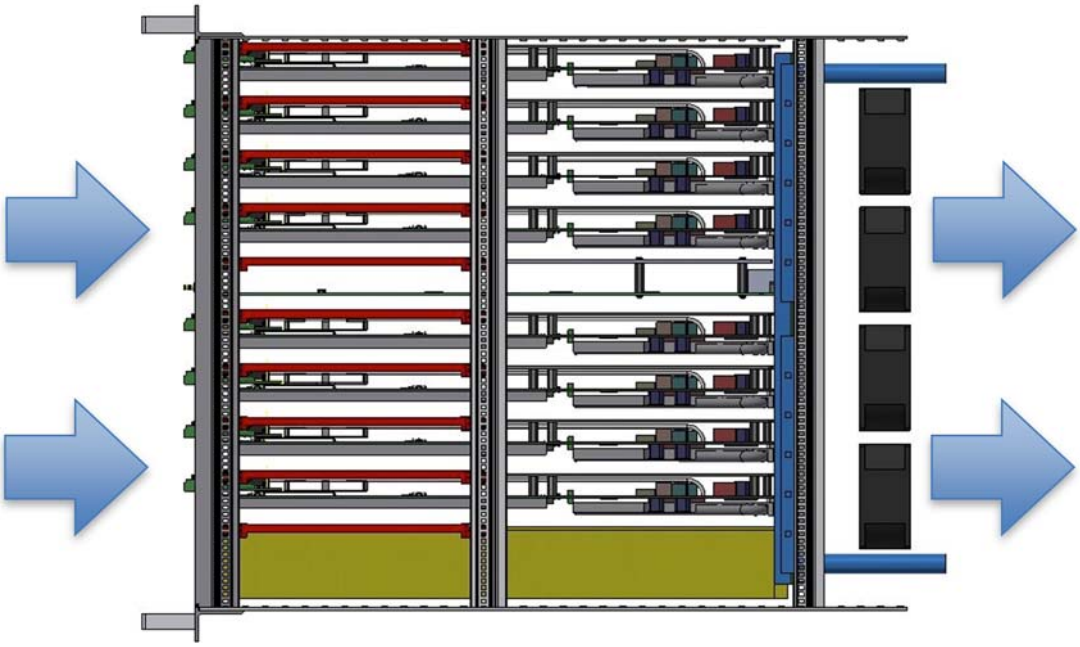


Figure 9-4 Sub-rack top view with air extraction, fresh air from front panel

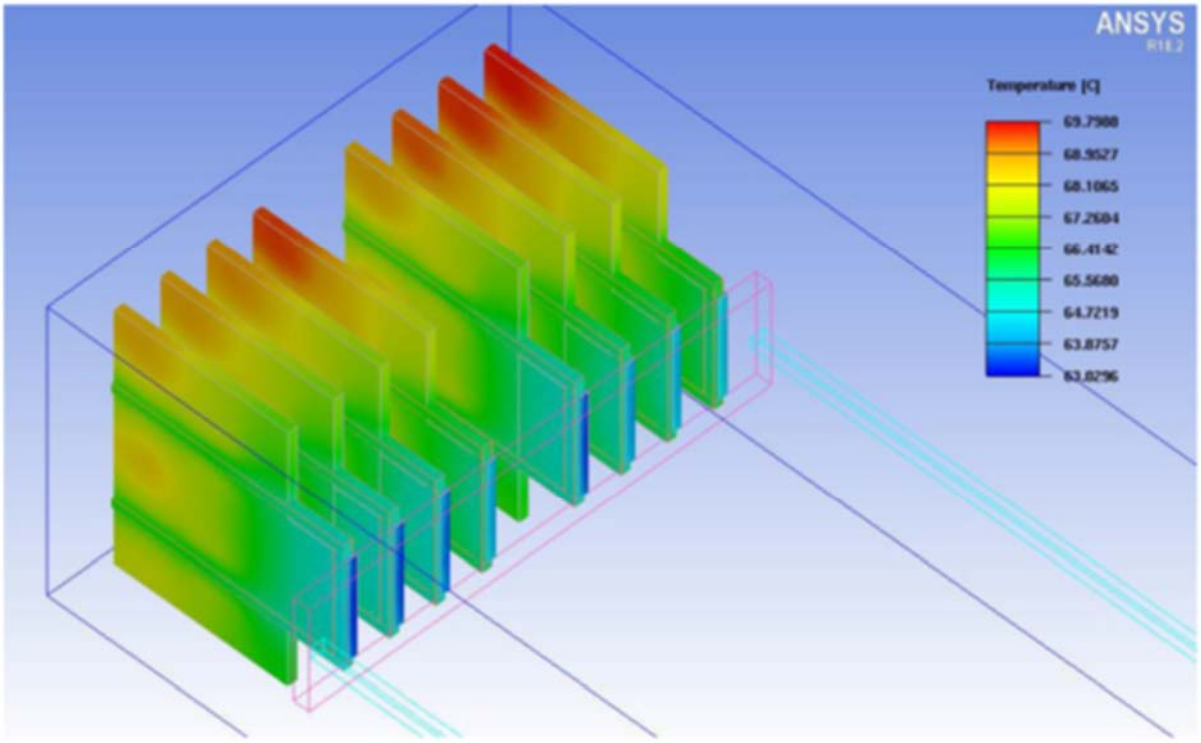


Figure 9-5 TPM Sub-rack thermal performance

While the heat flows from the board to the liquid circuit, the slowest transferring area will be the silicon interface material placed in between the heatpipe system and the liquid cold plate. Even if the rest of the cooling system is extremely efficient, the silicone pad will present a ΔT way higher than the heatpipes and the LCP. The right thickness of that pad (1.5mm) has been chosen to maintain the final temperature of the hottest component (FPGA) less than 70°C.

Due to the margin kept by assuming a liquid inlet temperature of 25 °C, the liquid cooling system has enough performances to cool the air in the sub-rack as well. Considering it is necessary to cool down an extra power from the rest of the circuitries we designed and additional heatpipe system to be mounted on top of the Liquid Cold Plate.
Fans installed on the rear of the sub-rack, allow to inject the right quantity of air.
Assuming an inlet ambient temperature of 40 °C, the air flowing in between the fins will be cooled down by the liquid flowing inside the Cold Plate. In the picture below can be seen the liquid cold plate with a constant temperature around 37°C cooling down the air inside the box of ≈ 3-4°C
More details can be found on [RD67].

9.4.1 LRU Thermal Performance

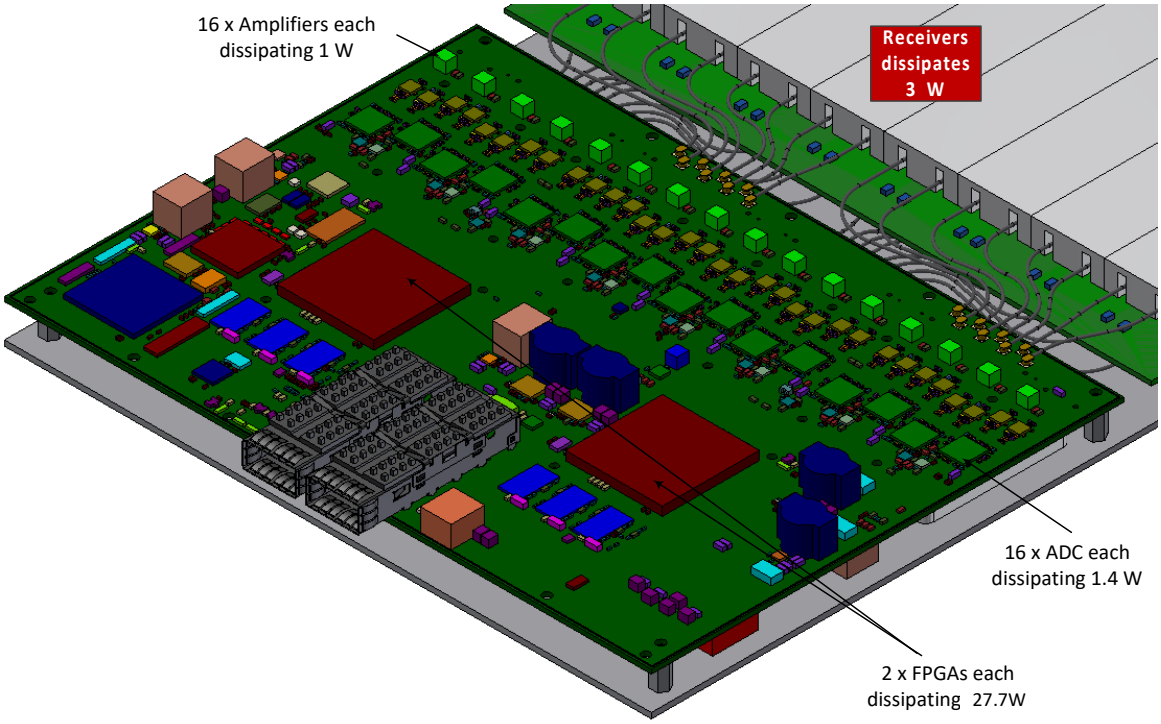


Figure 9-6 Main component dissipating on board

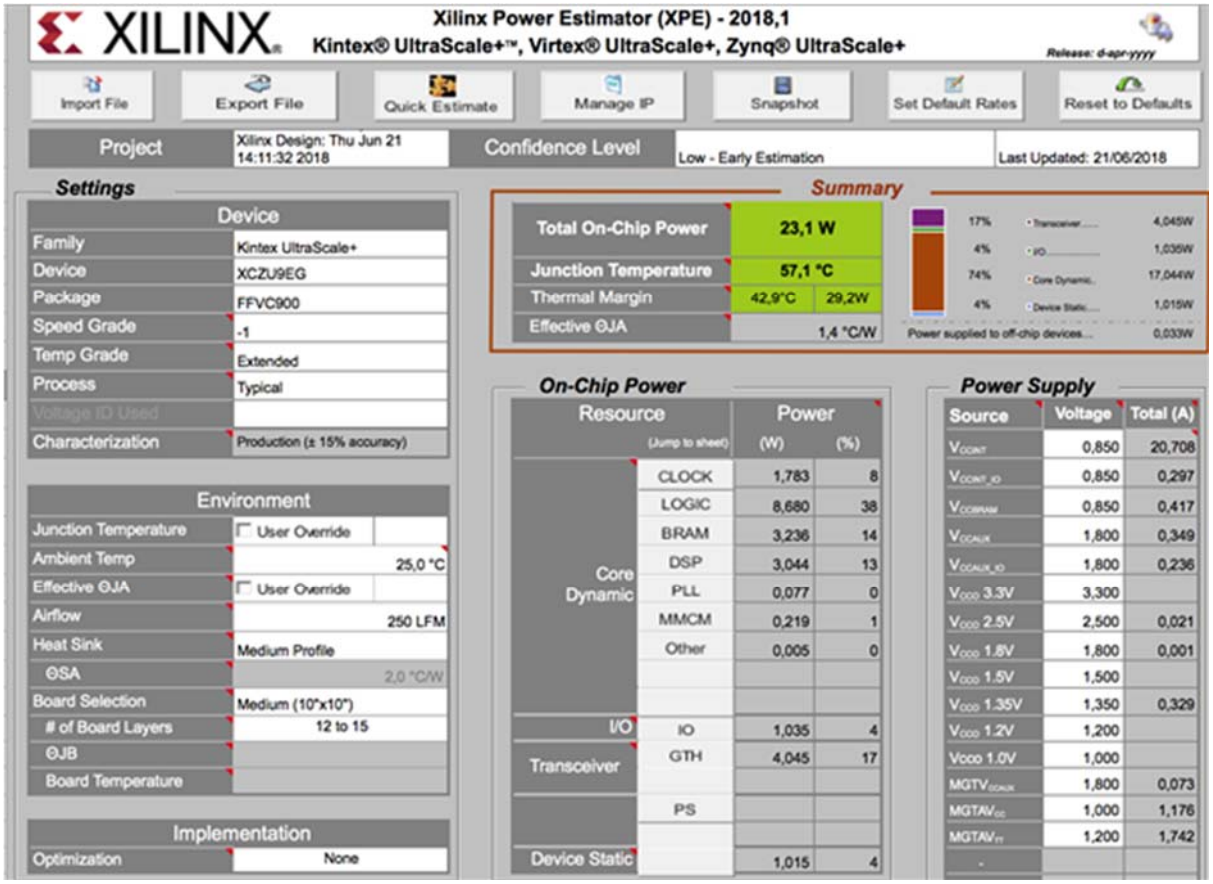


Figure 9-7 Xilinx FPGA Thermal Model estimation

The TPM power estimation is based on the test measurement on the revision 1.2 prototype, and successive design analysis as detailed in the following paragraphs.

The relevant power absorption, variable in the TPM design, is the power requested by the FPGAs, related to the loaded application and the incoming data.

The producing company, Xilinx inc., provides a spreadsheet-based power model, Xilinx Power Estimator, that can be loaded directly from the FPGA design tool, with detailed information generated by the design itself and edited manually, for estimations (i.e. clock speed variation power impact analysis) or post implementation fine tuning (i.e. data related information not considered in the FPGA design phase, as toggle rate).

The TPM AAVS1 FPGA detailed power design information, captured back by the design tool, has been imported in the spreadsheet to create a design model that is compliant with the measured absorbed power. This spreadsheet has been manually completed with the real operative condition that impact on the absorbed power, for example the clock speed, the data toggle rate, the effective supply voltages.

A relevant and unexpected feedback from the AAVS1 field test, has been observed.

The ADU-TPM design, running with synthetic RF input stimuli, requests about 130 Watt.

For the same FPGA application, executed in real operative conditions on AAVS1 field, the power dramatically increases to more than 150 Watt. This has been justified with the noise signal dynamic, that has a relevant impact on the total FPGA internal toggling rate. To manage the situations and maintain the power within the original limit some optional functions have been removed from the design, thus the power model of the design has been updated with the AAVS1 real measured field data.

This information has been moved manually in the new TPM 1.5 FPGA spreadsheet power model, that has been updated following the change of FPGA family, from Ultrascale present in the TPM-ADU

revision 1.2 to Ultrascale+, present in the future TPM-ADU 1.5. The two FPGAs are similar, they preserve the internal structure with light changes but the newest is built with newer silicon transistor technology (from 20 nm to 16 nm). Consequently, it is expected that the power model can be ported with a small error.
The main architectural updates at board level design of the new TPM-ADU 1.5 board revision are the memory interface (from DDR3 to DDR4) and the bus between the two FPGA (from parallel LVDS to high speed serial). The related FPGA power model has been updated manually to include also these changes.
In the end it is noted that the Xilinx company has updated the available FPGA power estimation spreadsheet recently; the previous version, used for the document submitted for the CDR, was an early revision (the related device was just released to the market). The new results are lower and has been reported as "Typical"; the previous values have been maintained as Worst case.

Component	T [C]	Location
FPGA	57.1	Junction

Table 9-5 LRU Thermal Modelling Results

9.4.2 preADU Thermal Performance

Considering the limited power dissipation by the RF circuitries installed on preADU board, the natural air flow convention allows to maintain the temperature under control by thermal transmission to the PCB and to the metallic lid that covers all devices. The cabinet cooling and fans have been designed considering also the aspect mentioned before.

9.4.3 Rack Thermal Performance

Cabinet power distribution design is based upon the TPM sub-rack preliminary design and the TPM cabinet design described in [RD12].
The TPM sub-rack preliminary design power model is summarised in the following table:

SUB-rack	Single Unit absorbed Power, Watt			Cabinet absorbed Power, Watt		
Element	Load	Typical	Maximum	Number	Typical	Maximum
TPM 1.5	DC 12	107,8	120	8	862	960
Sub-rack Management	DC 12	22	30	1	22	30
Sub-rack backplane	DC 12	5	5	1	5	5
Sub-rack FAN	DC 12	10	20	4	40	80
Power Supply, off 94%	AC220V	29,5	34,5	2	59	69

Table 9-6 Evaluation of the Sub-rack cooling budget

The sub-rack absorbed power is expected to be transferred mainly directly to the liquid through the TPM heatpipe and the backplane liquid cold plate air radiator; it is expected that only about 15% of the generated power will be transferred to the cabinet internal air.
All the other cabinet elements will be directly cooled by air, due to the expected limited absorbed power.
The total power directly transferred to the liquid will be about 3.740 Watt and the remaining 1.440 Watt will be transferred to the air. This estimation is function of the final temperature working point that will be chosen for the various elements present in the cabinet, mainly TPM FPGA temperature,

sub-rack cold plate temperature, sub-rack internal liquid flow speed and cabinet internal air temperature.
The cabinet shall be a close system also w.r.t. the cooling. The LFAA buildings (central and remotes) will provide a liquid circuit to each rack from the floor, dimensioned to meet the total cabinet absorbed power.

	Single Unit absorbed Power, Watt			Cabinet absorbed Power, Watt		
Element	**Load**	**Typical**	**Maximum**	**Number**	**Typical**	**Maximum**
TPM sub-rack	AC 220	988	1144	4	3953	4576
Cabinet Management	DC 24	25	33	1	25	33
Cabinet auxiliary	DC 24	100	200	1	100	200
Cooling system	DC 24	434	620	1	434	620
40G Switches	AC 220	200	500	2	400	1000
TOTAL LOAD, AC					**4912**	**6429**

Table 9-7 Evaluation of the Cabinet power budget

The worst-case scenario has been defined assuming the maximum power allocation to each single cabinet elements that shall be respected in each functional condition as design specification.
The typical is the target operative condition that has been estimated upon the current test done on the AAVS1 site and cabinet design analysis.
The cabinet liquid circuit specification is summarised in the Figure 9-8.
The infrastructure cooling liquid is interfaced with a cabinet liquid-to-liquid heat exchanger with two valves for possible isolation. The liquid-to-liquid cabinet exchanger allows the required isolation between the cabinet internal liquid circuit and the external one. The internal circuit shall be managed with a dedicated circulator to fix the flow speed of the liquid. The liquid–to- liquid heat exchanger shall be able to transfer all the expected cabinet power dissipation, with a (140 %) margin with a maximum temperature difference of 5-8 °C in the typical expected load configuration (7 KW liquid to liquid heat exchanger has been proposed).
The cabinet internal liquid shall be pure water. The sub-rack cold plates are alloy based and due to this fact possible galvanic current shall be evaluated to avoid metal corrosion inside the cooling circuit. The other materials allowed in contact with the cooling water are stainless steel and plastics.

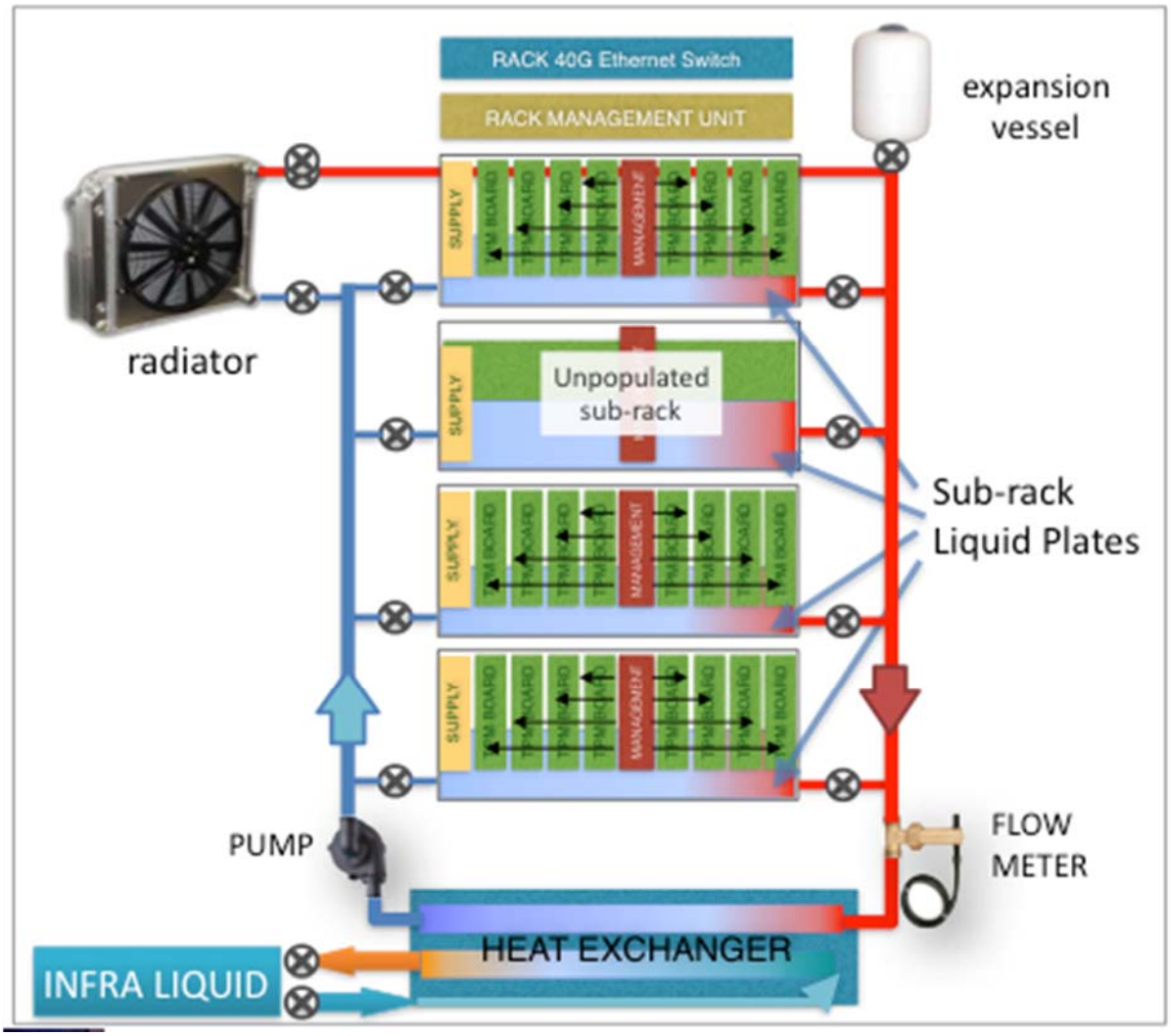


Figure 9-8 LFAA Cabinet liquid cooling circuit, main elements

9.4.4 Considerations of temperature fluctuations inside the cabinet and possible effects on electronics

We have 3 variables in the cooling system:

9.4.4.1 *Heatpipes*

the oscillation of power transferred through the heatpipes is of the order of tenths of a degree therefore does not affect the performance of the system.

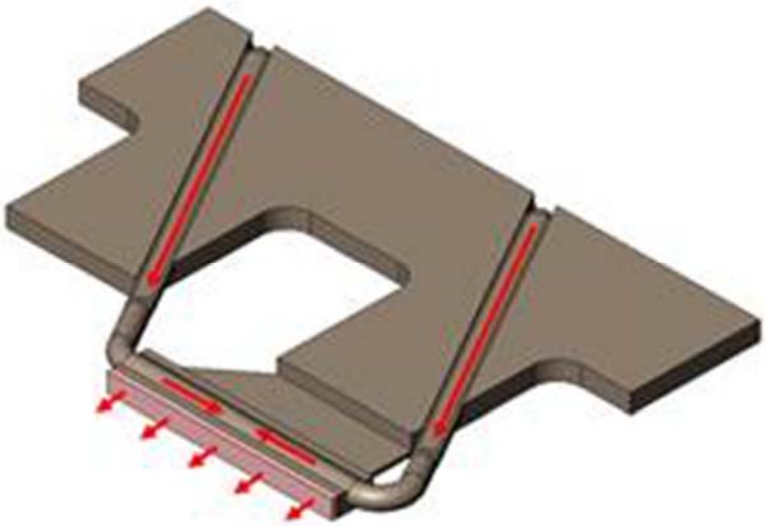


Figure 9-9 Heat flow in the heatpipe system

9.4.4.2 *Air temperature coming from inside the cabinet*

The cooling system works in terms of ΔT so if the temperature inlet of the air were to increase, it would also increase the output downstream of the heatpipe system mounted on the liquid cold plate. The amount of heat passed to the liquid will be the same but the temperature in the cabinet will be greater and this could have a negative effect on the performance of the electronic boards both in terms of duration, both in terms of efficiency (and therefore power to dissipate).

- The temperature inside the cabinet must be monitored and maintained. Any slow change will affect the whole cooling system.
- It is important to make the air path between fans, fins and outlet holes as free as possible.
- Any fluctuations in the air intake temperature will not cause significant air changes inside the subrack because the air density will not change perceptibly.

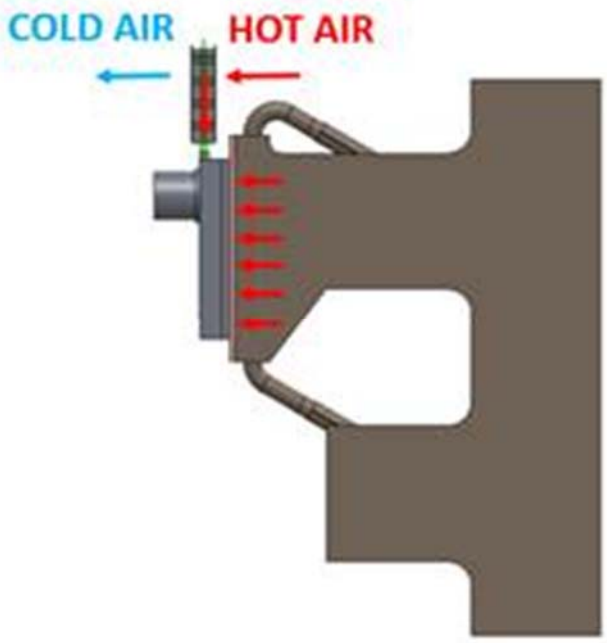


Figure 9-10 Heatpipe- coldplate interface

9.4.4.3 *Temperature of the liquid coming from the Chiller:*

The water-water exchanger also works in terms of ΔT, so if the temperature of the liquid coming from the Chiller oscillates, the operating temperature of the cabinet cooling circuit will also fluctuate. In any case, the liquid temperature at the inlet of the hydraulic circuit is constant by specification. In case of malfunction (but in this case it will be signaled in some way by the Cabinet monitoring board) and important changes in the temperature of the liquid coming from the Chiller can cause a reduction in viscosity with a consequent reduction in pressure drops.

	WATER 25 °C		WATER 35 °C		WATER 45 °C	
OUTPUT	Dynamic Viscosity - μ - (kg/m-s)	0.00091	Dynamic Viscosity - μ - (kg/m-s)	0.00075	Dynamic Viscosity - μ - (kg/m-s)	0.00061
	Density - (kg/m^3)	997	Density - (kg/m^3)	994	Density - (kg/m^3)	990
	Specific Heat - c_p - (J/kg-K)	4182	Specific Heat - c_p - (J/kg-K)	4176	Specific Heat - c_p - (J/kg-K)	4172
	Cinematic Viscosity - ν - (cSt)	0.982	Cinematic Viscosity - ν - (cSt)	0.807	Cinematic Viscosity - ν - (cSt)	0.663
	Thermal conductivity - W/mK	0.666	Thermal conductivity - W/mK	0.677	Thermal conductivity - W/mK	0.685

Figure 9-11 Physical properties of the cooling liquid vs temperature

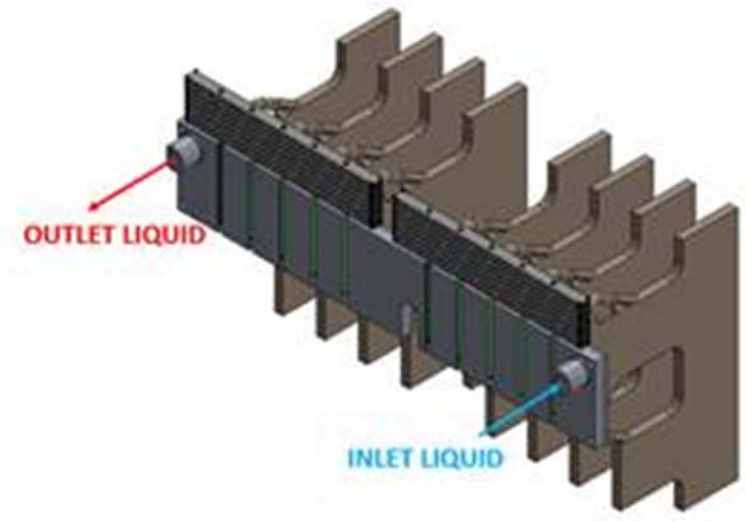


Figure 9-12 Cold plate liquid ingress

Having assumed the foregoing, it can be concluded that, from a preliminary analysis, in the case of normal operation the temperature variations inside the subrack and, in particular, on the electronic boards that house the optical-electric transducers, RF circuits and ADC systems, can be considered as a first approximation constant.
Having said this and confirmed that the temperature is constant, the relative gain variations over time of the components will be negligible. In any case, during the next phase and after prototyping, being more aware of these thermal aspects, we can better evaluate if the effect of temperature fluctuations inside the cabinet is an important and critical aspect for the system.

9.5 Electrical Performance

From the Table 9-7 the maximum power required by the cabinet is 6429W.
The subrack and cabinet management boards power estimation were performed with measurement of the absorbed power of the first prototypes. Small changes on the final revision and management applications may have an impact but we don't expect a large spread from these values.

The cooling power estimation comes from the design presented in the Cabinet preliminary design [RD68], coming from AAVID Thermalloy. The main power request comes from the four liquid circulators, remotely PWM controllable by a cabinet management application, to obtain the requested liquid speed in the cooling circuit. This estimation considers placing all the four circulators at the 60% of the available capability (max 80 Watt each), corresponding to the expected working point from a preliminary pressure drop design. The other main power allocation is for the cabinet internal air fans, placed on the radiator, that has a preliminary budget of 200 W (max 300 W). A power request from the circuit sensor has been added too (about 2 W each).

For the 40G switch, a selected commercial item has been considered that satisfies all the cabinet requirements (Arista 7050X3). From the component datasheet the absorbed power can move from about 150 Watt up to 500 Watt for the full speed usage. These switches can perform up to 32 channels at 100 Gbps speed each; for LFAA application they are only partially used with 20 interfaces running at the speed of 40 Gbps. As consequence preliminary budget of 200 Watt, close to the minimum, has been allocated. This analysis shall be verified on the final device in the real operative conditions.

A cabinet auxiliary supply, DC 24V, is needed for the power distribution circuit itself and for the cabinet management board, that controls the cabinet power on sequence. This supply powers the remote-control switches and the other power distribution elements, described in the cabinet description document.

Current cabinet power distribution scheme is summarised in Figure 9-13.

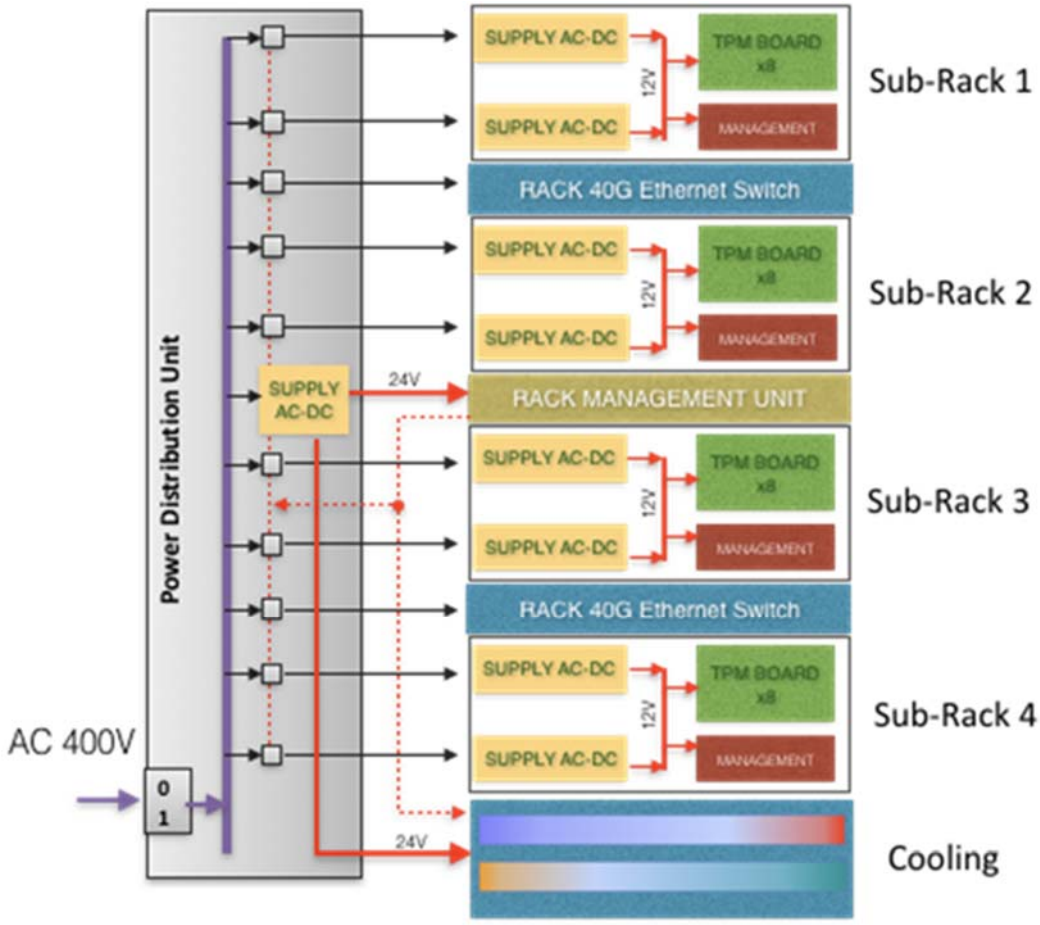


Figure 9-13 LFAA Cabinet power distribution scheme

The violet input line represents the three-phase input supply. After the manual input switch, the internal phases are distributed as single phases to the several elements, black lines. The DC supplies are red line (24V at cabinet level, 12V at subrack level).
The 32 TPM are organised in the four subracks that also integrate the management boards. Each subrack currently is designed with two redundant single AC phase power supplies (PET1300-12-054xA) with 12V DC output joined together in the backplane ([RD85] sub-rack feasibility study). These two devices are capable of 1300 Watt each, 108 A, with maximum efficiency of 94% at half load.

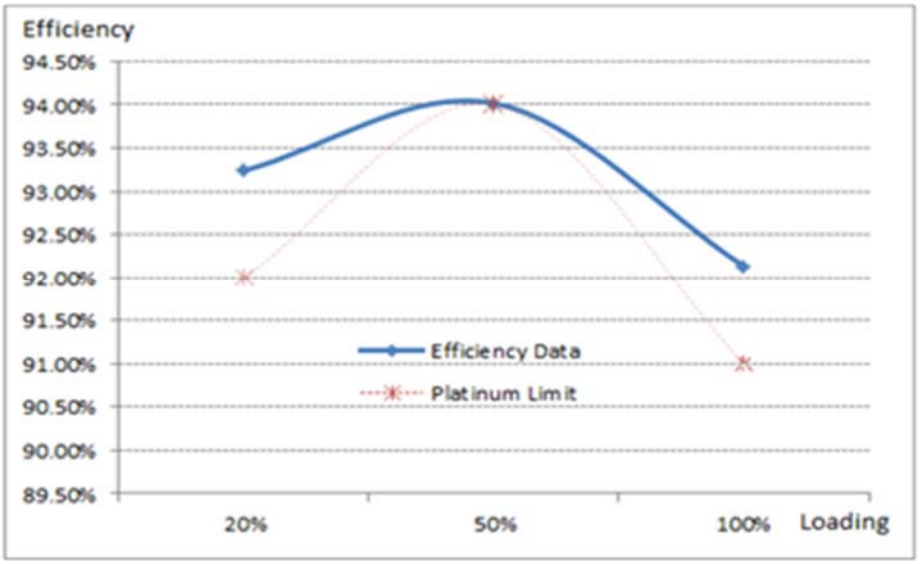


Figure 9-14 PET 1300 efficiency measurement curve

In normal condition they work together at about 40% of their maximum capacity, close to the efficiency peak. In case of single failure, the load can be raised to 80% without functional limitation.
Phase unbalance may occur only if one sub-rack power module is active.
These power supply modules are remotely managed by the subrack management board and several parameters (PET1300-12-054xA datasheet) can be monitored.
The 12V output of each module is connected to the subrack backplane where the power is distributed to the subrack management board (always on) and to each TPM (sub-rack preliminary design) but controlled and monitored by a special IC that can switch ON/OFF the TPM, monitor the absorbed [RD85]An auxiliary 24VDC is needed to power the rack management unit and the power distribution elements itself. This units shall be always powered ON after the startup.
The cooling system is currently supplied with a dedicated 24VDC circuit with two main loads, the four pumps and the radiator air fan.
The 24V power unit can be separated to balance the load on several AC phases.

9.5.1 AC Phase Load Balancing

A preliminary phase allocation of the cabinet current load is summarised in the following table:

Element	Power, Typ	Power, MAX		Phase 0	Phase 1	Phase 2		Phase 0	Phase 1	Phase 2
Subrack half load 1	494	572		494				572		
Subrack half load 2	494	572			494				572	
Subrack half load 3	494	572				494				572
Subrack half load 4	494	572		494				572		

Subrack half load 5	494	572			494				572	
Subrack half load 6	494	572				494				572
Subrack half load 7	494	572		494				572		
Subrack half load 8	494	572			494				572	
40G Switch 1	200	500				200				500
40G Switch 2	200	500			200				500	
Aux AC-DC 24V	100	326,5		106				326,5		
Cooling AC-DC 24V	434	620				462				620
TOT AC 400V	4.922	6.523		1.589	1.683	1.650		2.043	2.216	2.264
Optimal phase load:	1.641	2.174								
Phase unbalance:				3,1%	-2,6%	-0,6%		6,1%	-1,9%	-4,1%

Table 9-8 Estimated System AC Phase Loading

All the power values are in Watt and it is assumed the target efficiency of the AC-DC converter of 94% to calculate the effective load of the system on the external supply.
Final numbers can be slightly different, so a fine tuning will be required on the final design to optimise phase balance.
Possible phase unbalance may occur only if some cabinet function were disabled.

9.5.2 Start UP sequence

The cabinet and the related element design allow a controlled and incremental start-up sequence and multi-level monitoring capabilities.
A possible start-up sequence is reported in the following table:

Step	Supply	Element supplied	Available functions	Requested power	Power %
0	None	None	None	0	0%
1	Aux AC-DC 24V	Management & AC PDS	Cabinet management	125	3%
2	40G Switch 1	40G Switch 1	Network connection to LFAA	325	7%
3	Cooling AC-DC 24V	Cabinet cooling	Cooling available	759	15%
4	Subrack 1,2	Subrack 1,2 management	Station 1 management	813	17%
4.1		Station 1 TPM	TPM management	1293	26%
4.2			TPM ready to run	1613	33%
4.3			Station 1 running	2735,8	56%
5	40G Switch 2	40G Switch 2	Network connection to LFAA	2935,8	60%
6	Subrack 3,4	Subrack 3,4 management	Station 2 management	2989,8	61%
6.1		Station 2 TPM	TPM management	3469,8	71%
6.2			TPM ready to run	3789,8	77%
6.3			Station 2 running	4912,6	100%

The cabinet shall be powered-on manually by a dedicated input switch. At the power-on, only the auxiliary 24V supply is active and the cabinet management board starts to operate.

The management board can be pre-programmed or remote-controlled to manage the start-up sequence. In the cabinet, the management board will control the power supply switches and configure and run the other boards by ethernet based commands.
As a first step, if requested, the management can power-on the first 40G switch supply to provide the connectivity with the LFAA network.
After that, the cooling circuit shall be started; the requested power in the first steps can be lower due to the cabinet partial power activation.
Then, the TPM sub-racks can be powered to start the station power-up sequence; a single sub-rack or all the four sub-racks can be activated together for a different power up scheme.
Powering a sub-rack, only the backplane and the sub-rack management board are powered and stars to operate in few seconds. The network function is available, and the sub-rack management can receive the ethernet base commands to proceed with the start-up or can be programmed for automatic start-up.
Each sub-rack TPM can be powered and verified for the absorbed current. When powered-on, the TPM provides only the management function, ready to be programmed. Also, the TPM internal power distribution is partially OFF. It is possible to power in the digital section and the analogue section separately; by default, at power-on only the management section of the TPM is powered with a small power consumption.
At this point, the management board can power-on the requested TPM sections and can program the FPGAs, set the working frequencies in the PLL, supply and configure the ADC and the optical receiver circuit. In these steps, the absorbed current can be monitored at backplane level and verified against pre-set values and in case of variations, an automatic shut-down can be programmed. If everything is fine, the TPM is ready to run. In the last step, the ADC and the VGA can be placed in the sampling mode to start the acquisition.
In the proposed cabinet power-on sequence, two stations are powered on separately, just to detail the system capability. It is possible to power-on the stations together with a different power sequence.

9.5.3 Shut down & voltage transient

The cabinet shall be designed to manage a controlled shutdown command and an undesired and unexpected input supply voltage transient, with respect to the power quality specification document.
Controlled shutdown means that the cabinet management board receives an ethernet based command and executes in reverse order the power up procedure, ending with the stand-by operation. In this case, it is expected that the normal communication with any other LFAA equipment has been stopped.
A voltage transient means that unexpected and temporary loss of input power will occur, and the cabinet shall perform pre-defined safe procedure to minimise loss of configuration data and the time required to recover in a fully operational state.
To manage this complex situation, some assumptions are needed, to be verified and confirmed:

- No cabinet complete auxiliary power unit shall be provided, due to the related absorbed current;
- The TPM shall not store data in non-volatile memory, with possible exception of the FPGA configuration bitstream and some pre-defined configuration parameters;
- The TPM can be powered off without controlled sequence; this implies the complete loss of data;
- The cooling circuit can be powered off without controlled sequence;
- The network switch can be powered off without controlled sequence, TBC;
- The cabinet configuration data will be managed by the management boards;

- The transmission of the cabinet configuration parameters from the MCCS and the TM to the cabinet will be done with a safe procedure, with acknowledge.

The cabinet management and the sub-rack management boards shall implement a safe shut down sequence to avoid loss of function and configuration data.
For both TPM unit and the management board, the input supply scheme is summarised in the following scheme:

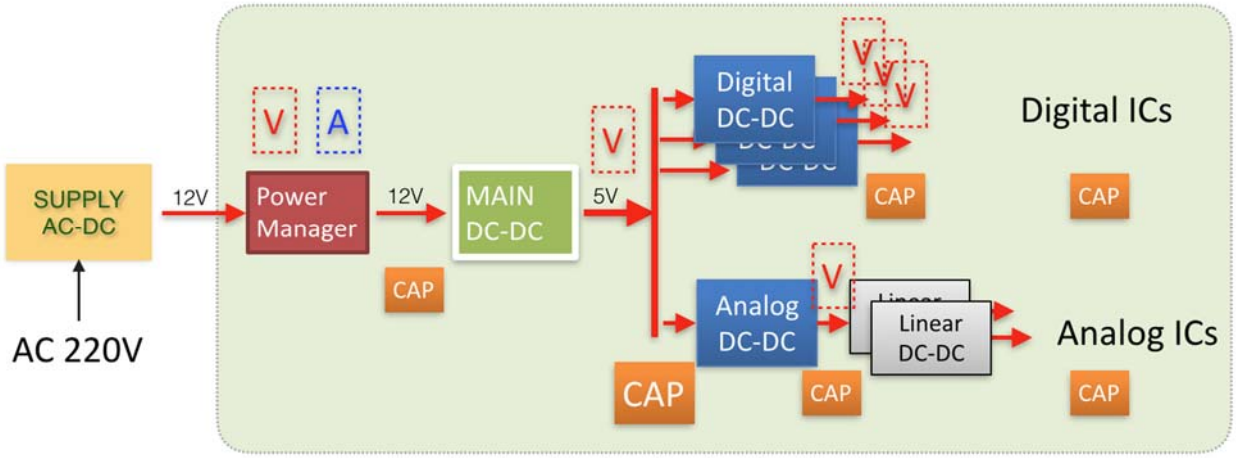


Figure 9-15 Power management scheme for TPM and management board

The input supply is monitored for voltage, and the absorbed current is continuously checked by the Power Manager circuit that implements the hot swap function overcurrent protection functions. This circuit can be remotely accessed by a serial bus and the measured values are available to the board level power management application.
The input supply is expected to be at least 12V and is transformed to a lower 5V by the single MAIN DC-DC that provides the current to all the other board elements. The 5V is monitored and several high capacity capacitors are present at this power distribution level.
All others DC-DC converters are connected to the internal 5V supply; they generate directly the supply for the digital circuits or an optimised supply for the linear regulators reserved for the analogue parts.
Each DC-DC circuit voltage output is monitored again by the management application.
With this architecture, a voltage transient in the input can be detected by the Power Manager before the failure can happen.
The transient duration and the board absorbed current might impair the behaviour of board functions.
In the management boards, to implement the safe shut-down, a new power manager function is proposed, to be scheduled in the next planned revision 1.1.

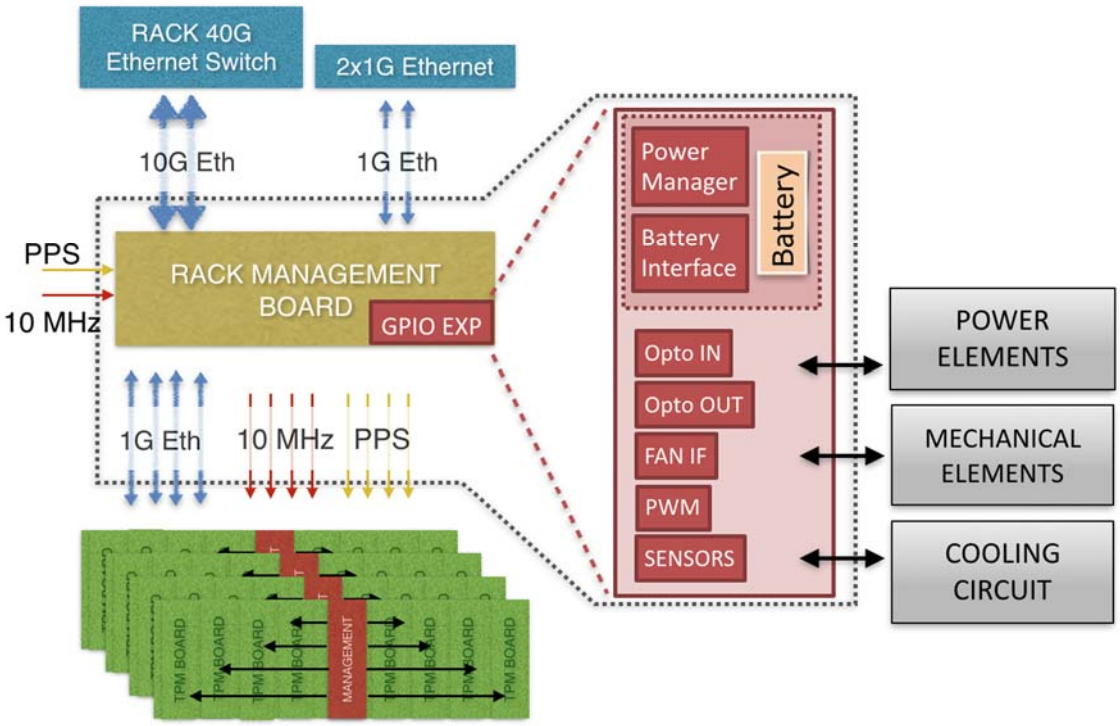


Figure 9-16 Timing and ethernet distribution at cabinet level

The new power manager circuit shall implement the following functions:

- Monitor the input voltage;
- Manage a TBD size internal battery;
- Generate an auxiliary supply to the management board if the input voltage drops below a defined threshold.

Considering that the requested power for the management board is quite reduced and the shutdown sequence will request about a minute, a medium-small rechargeable battery shall be enough to implement different possible transient scenarios.

The management board shall implement the following software procedure:

- The OS shall be executed in the dynamic RAM memory, the sensitive data shall be stored in a protected non-volatile memory, updated with a safe procedure;
- All configuration data, transmitted by the external control application, shall be stored in a non-volatile memory.

In the management board, a power management service shall be always active to monitor the input voltages and, in the sub-rack configuration, the AC-DC status register.

The management service shall implement a timer to execute a safe OS shut down procedure, accordingly with the battery capacity.

In case of anomalies, the internal DC supply of all configured elements shall be monitored to determine if a reconfiguration is required when the supply returns to the nominal ranges.

It is also possible to halt the main TPM functions, powering down the analogue circuits that require poor configurations data and execute a fast restart procedure in case of short transients, without reconfiguring the FPGAs.

Several shut down scenarios can be identified, corresponding to the supply input type:

- Short transients that do not cause loss of configuration or loss of function, to be monitored;
- -Short - medium transients that cause TPM loss of function and configuration

- Medium transients that cause the shutdown of all elements except of the management boards, which can possibly maintain a fully operative condition;
- Long transients, that cause the shutdown of the management board.

Different restart times and operations are involved, and these shall be defined together with the cabinet remote software control interfaces.

9.6 SPS Rack Single Line Diagram

The Single Line Diagram (SLD) for each Signal Processing Cabinet is shown in Figure 9-17 below:

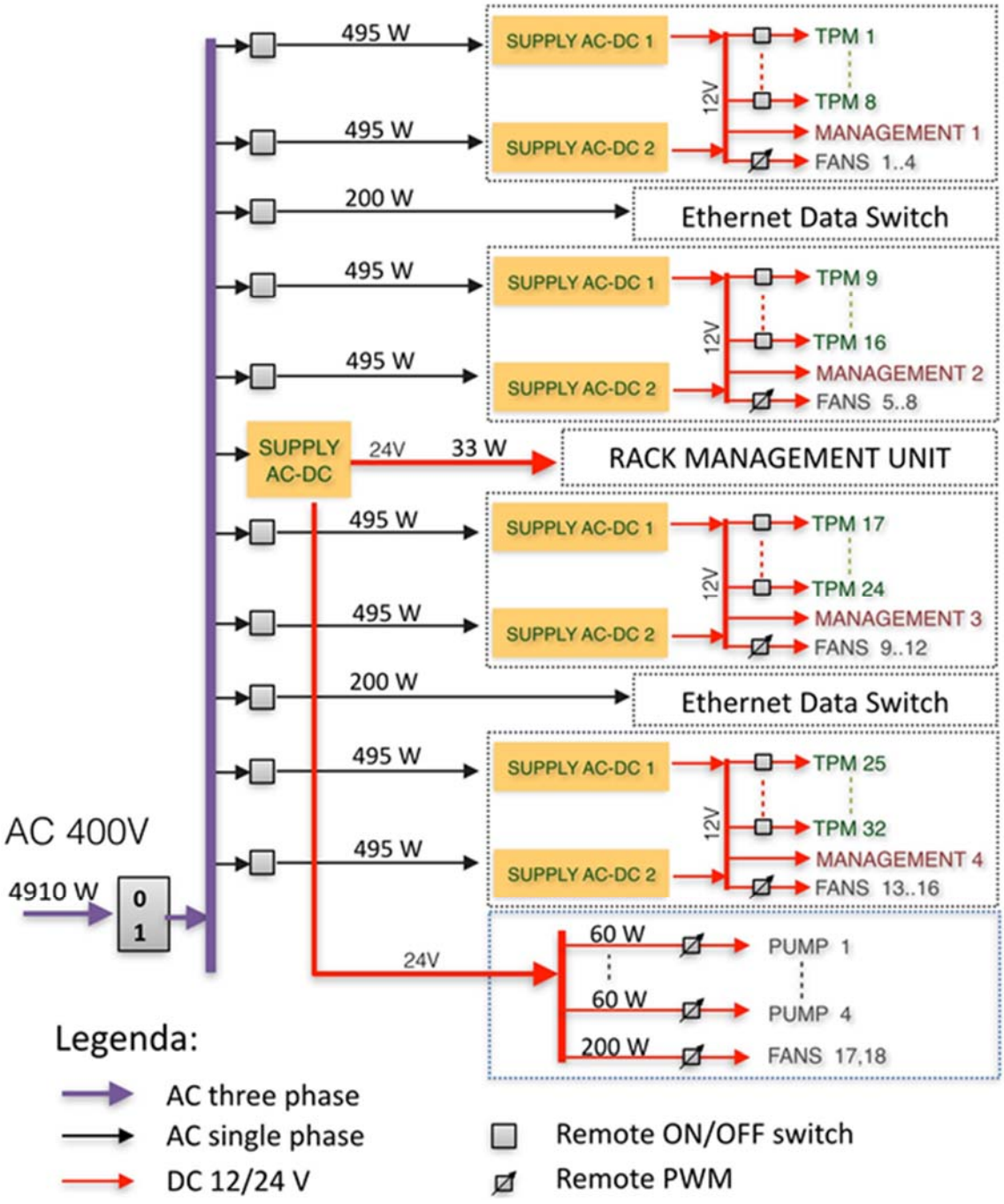


Figure 9-17 SPS Rack SLD

The input block includes several elements: manual switch, a magnetic protection for short circuit, and electromagnetic noise suppression block.
Each ON/OFF switch and remote PWM control include the over-current safety protection. The management boards are always powered directly, and their input power supply interface provides an integrated safety over-current ON/OFF switch.
The absorbed power is a preliminary estimation with different components: the power absorbed by the TPM has been calculated starting from the current board revision, while the power of the other elements has been only estimated based on the expected operative conditions and their maximum power consumption.
The power efficiency of the power supply has been assumed 94%, based on the one that has been identified for the sub-rack.

10 Reliability Availability and Maintainability

SPF is allocated an Inherent Availability (Ai) of ≥ 99.99% and a Mean Time to Repair (MTTR) of 1 hour in the SKA RAM Allocation document [AD31]

This section provides the rationale and analysis to show that LFAA.SPS meets the allocated Ai and MTTR.

10.1 Reliability, Availability Maintainability Allocation

10.1.1 Design for Reliability

LFAA.SPS's reliability and robustness are increased with measures such as:

1. Selection of high reliability components (where cost-effective).
2. Design to have the fewest possible components for required functionality.
3. Design to have the fewest possible variations of equipment types and configurations
4. Design of built-in tests (see Section 6.9) and advanced diagnostics (see Section 13) that have complete board coverage (i.e. to sense all component failures).
5. Use of components that have plug and play modularity for rapid part replacement (see Section 5.4.1).

LFAA.SPS reliability is further enhanced by:

6. Ensuring a dust free/clean facility cooling air supply (INFRA to LFAA ICD [AD35]).
7. Ensuring that facility cooling is enough to keep equipment within temperature limits (via thermal analysis and the use of advanced cooling techniques, see Section 10.4).
8. Proactively replacing parts with failure rates that increase over time (parts that mechanically move), such as TPM Sub-rack cooling fans and AC-DC power supplies (that have cooling fans and failure-prone AC-input electrolytic capacitors).
9. Ensuring that facility power doesn't exceed equipment EMC limits (ESD, voltage dropouts, transients, and surges as well as harmonic distortion; see the INFRA to LFAA ICD [AD35].)

Note that LFAA.SPS operates in a benign temperature-controlled ground environment specified in the INFRA to LFAA ICD [AD35]

10.1.2 SPS RAMS Product Breakdown Structure

Table 11-1 below provides the relevant parts of the SPS Sub-element Product Breakdown Structure (PBS) as they apply to RAMS (CP = Control Processing, SP = Signal Processing). The "Level" column indicates the hierarchy of each item in the PBS. The Sub-element hierarchy consists of assemblies, sub-assemblies, and finally components (not indicated in this PBS) at the lowest level. LRUs are items that must be removed and replaced at the organizational level (O-Level or 1st level) to restore the Sub-element in case of a failure.

PBS Level	Name	Product Structure	#	MTBF Estimate	MTTR Estimate	Repair-able?
1	Signal Processing System	Sub-Element (CI)	1	-	-	Y
2	Cabinet Chassis	Bulk	256	-	-	Y

PBS Level	Name	Product Structure	#	MTBF Estimate	MTTR Estimate	Repair-able?
2	Patch Panel	Bulk		-	-	Y
3	Cabinet Fans	LRU	1024	80000	35	N
3	Cabinet Cooling	Assembly	256	500000	125	Y
3	Cabinet Piping and Valves		256	500000	25	N
3	Cabinet PDU		256	1000000	30	N
3	Cabinet Management Board	LRU	256	264500	90	Y
3	TPM Subrack Assembly	LRU				Y
4	Sub-rack cooling	Assembly	2048	100000	125	Y
4	Sub-rack Power Supply Unit		2048	80000	30	N
4	Sub-rack Management Board	LRU	2048	264500	30	Y
4	Tile Processing Module Assembly	Assembly				Y
4	100 G Ethernet Data Switch (32ports_)	LRU	512	160000	55	Y
5	Optical Rx	Bulk	131072	3054942	60	N
5	Pre-ADU PCA	Bulk	15384	1514698	60	Y
5	ADU PCA	Bulk	16384	250000	90	Y

Table 10-1 SPS Equipment MTBF (h) and MTTR (min)

10.1.3 Reliability Prediction

The reliability (MTBF) and repair time (MTTR) estimates for each assembly and sub-assembly are as indicated in Table 10-1. The MTBF estimates of COTS equipment are from device datasheets (actual or similar devices) and from experience using similar products.
The MTBF of the bespoke boards are calculated using the Telcordia SR-332 reliability prediction procedure for electronic equipment. The board's Bill of Materials (BOM) contains the parts list that is used to predict the board's MTBF.)
MTTR allocations for COTS and bespoke items are engineering estimates to be confirmed during the construction phase as part of maintainability analysis.
Bespoke LRU production units are screened using Highly Accelerated Stress Screen (HASS) tests to reduce the risk of delivering units with infant mortality issues (not predicted by the reliability models) to the site.

10.1.4 Operationally Capable

Operationally Capable (OC), for the SPS, is defined when enough processing resources are available to process ≥ 95% of the telescope's receptor data to obtain 95% of data products. SPS is designed to have an Ai ≥ 99.99% while being OC.

10.2 Availability and Maintainability

The SPS inherent availability model is provided in this section.

10.2.1 TPM LRU

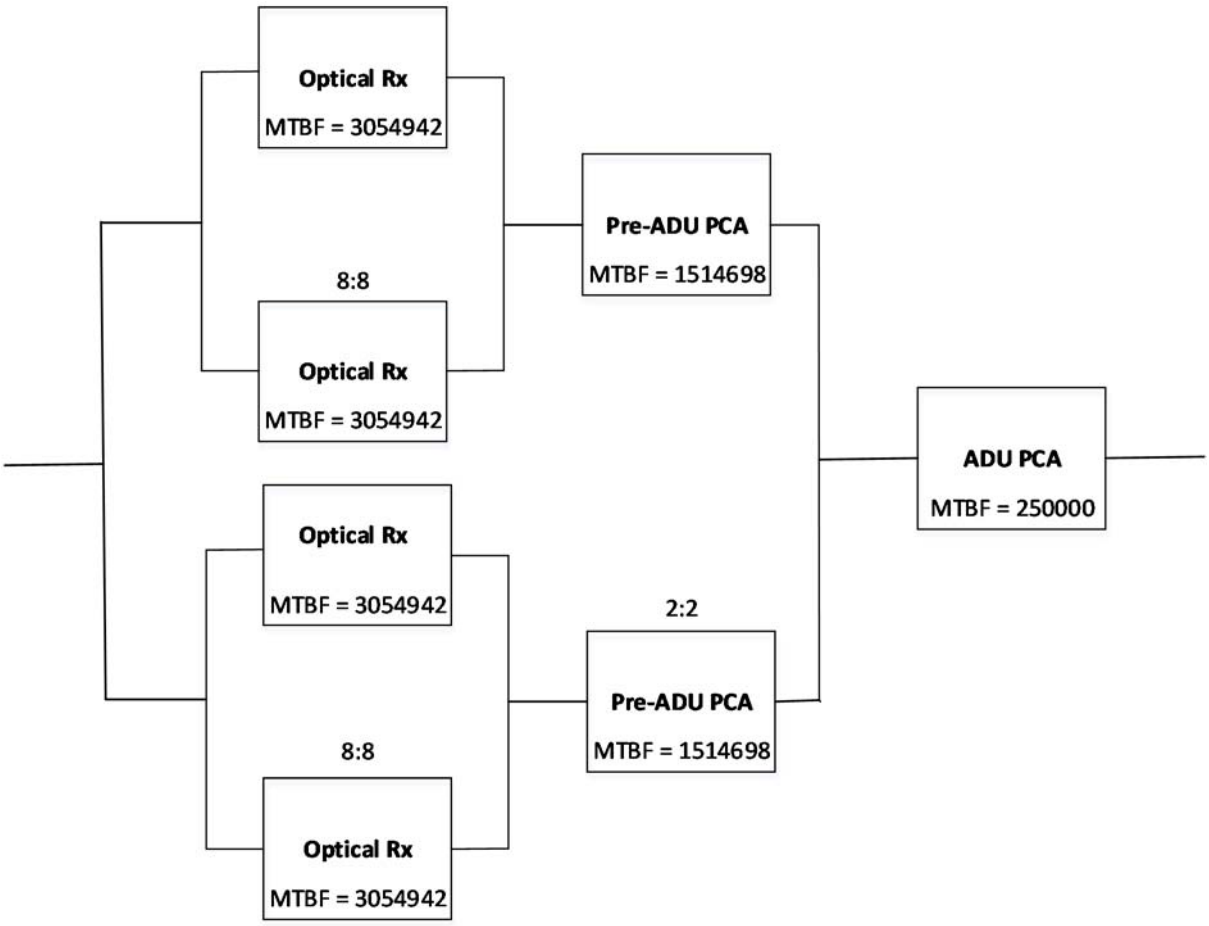


Figure 10-1 TPM reliability block diagram

10.2.2 LFAA SPS Sub-rack

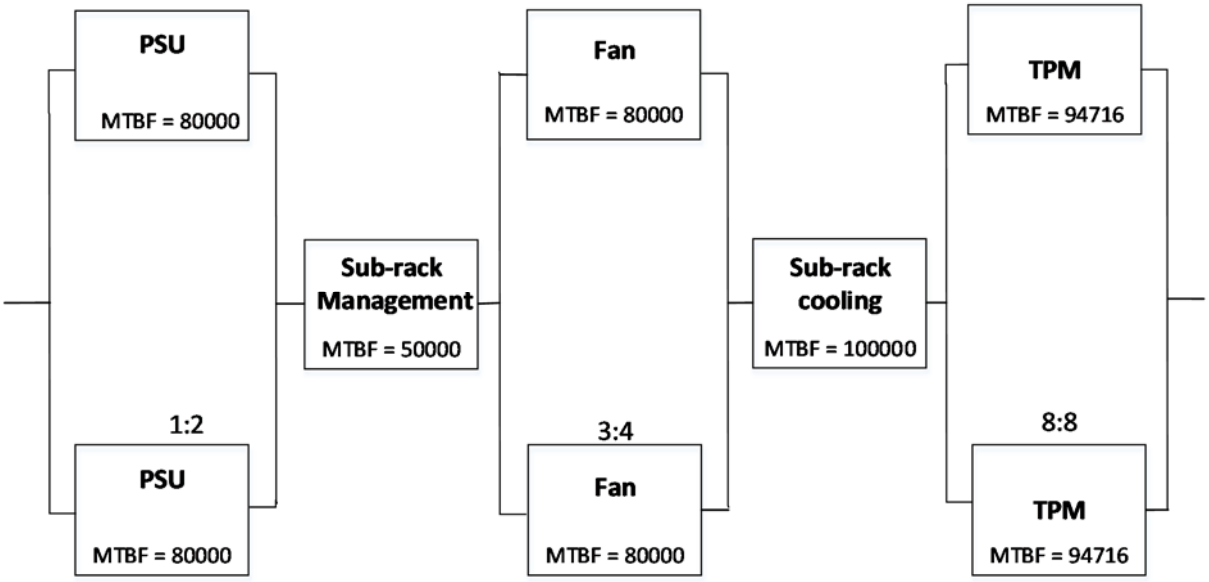


Figure 10-2 SPS TPM Sub-rack reliability block diagram

10.2.3 LFAA SPS Cabinet

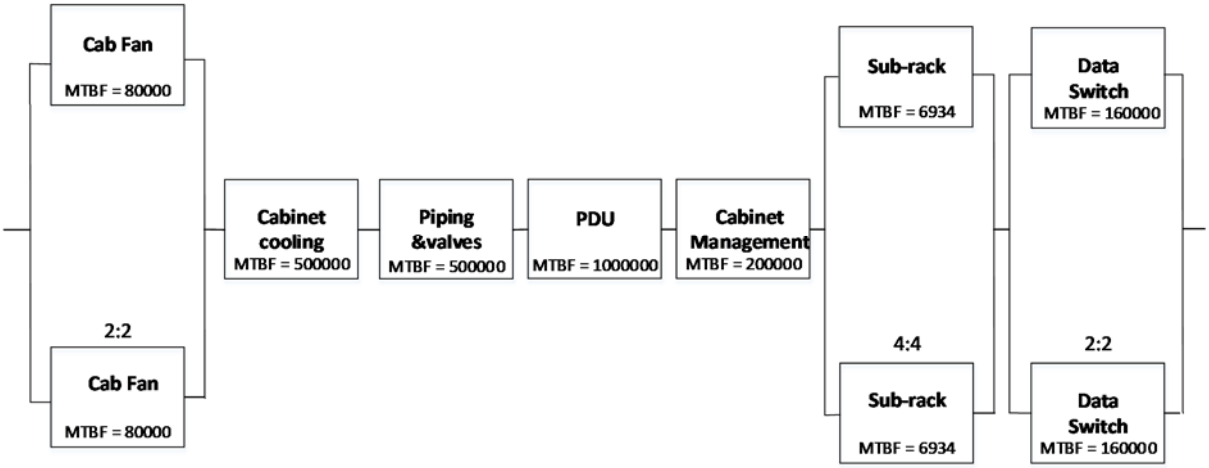


Figure 10-3 LFAA SPS Cabinet reliability block diagram

10.2.4 Muxponder



Figure 10-4 Muxponder Reliability block diagram

10.2.5 LFAA outer RPFs

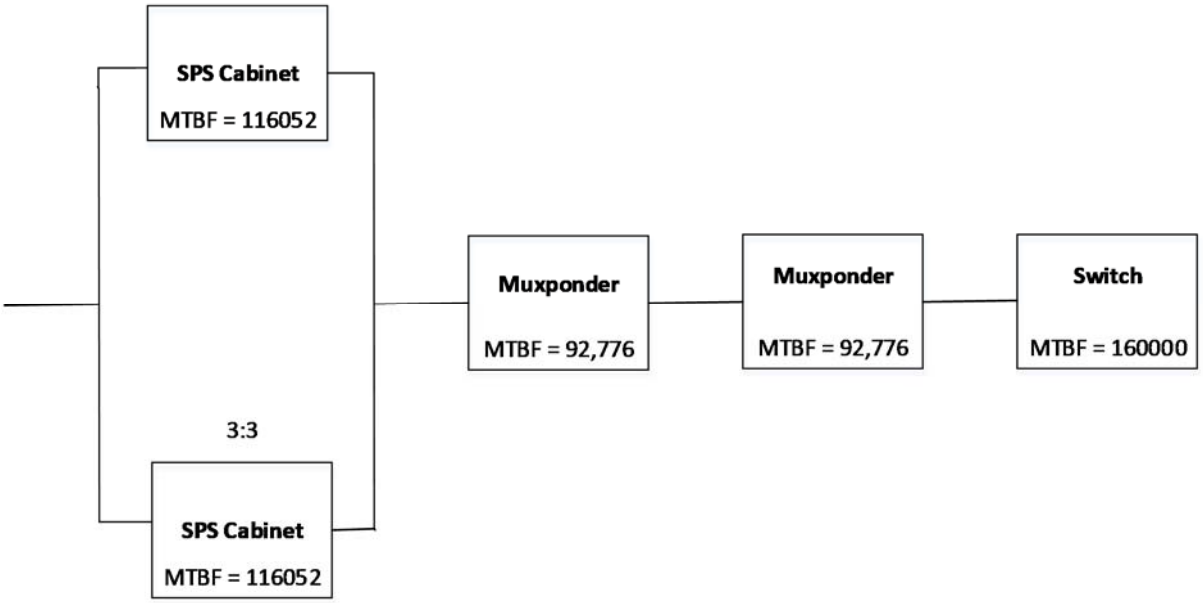


Figure 10-5 LFAA outer RPF reliability block diagram

Figure 10-5 Shows the worst-case signal chain for reliability. This is where extra equipment is used to ensure the signal can be transmitted over the distances for the outer ten RPFs. In this case there is a muxponder at the RPF and one at the CPF for each of the outer ten RPFs. A switch is also in series as this converts from 100 G bit/s links to 40 G bit/s links required by the CSP equipment.

10.2.6 LFAA.SPS Sub-Element

The reliability for the SPS Sub-Element is effectively "k out of n scenario" with 256 SPS cabinets in parallel delivering 512 beams. Greater than 95% of these cabinets need to be operational at any one time i.e. ~244 cabinets. Given the MTTR is nominally 1 hour, then the probability of twelve cabinets simultaneously failing in the same one-hour period is infinitesimally small which means the availability is very close to one.

Item	Inherent Availability	MTBF(h)	MTTR(h)
Optical Receiver	~1	3054942	1
Pre-ADU	0.999999	1514698	1
ADU	0.999994	250000	1.5
Tile Processing Module	0.999987	94716	1.19
SPS Sub-rack	0.999846	5541	0.85
Muxponder	0.99999	92766	0.91
SPS Cabinet	0.99947	1602	0.85
Outer RPF	0.99839	526	0.88
SPS Subsystem	1	∞	0.85

Table 10-2 SPS Inherent Availabilities

LFAA.SPS's calculated Ai, for 95% operation capability is ~ 1, more than the required 99.99% (L3-111).
LFAA.SPS's calculated MTTR is 0.85 hours at O-Level, less than the required 1 hours (L3-114).
Provided the estimations and allocations of Table 10-2 are approximately correct, LFAA.SPS meets its Ai and MTTR requirements.
Ignoring the operational capability and considering the MTBF for 100% of the SPS equipment, the mean time between any item in the SPS failing is ~ 6.2 hours which is nominally equivalent to, on average, 117 failures per month. Given the MTTR for the SPS subsystem is 0.85 hours, then the Direct Maintenance Hours per month is ~ 99 which is well within the allocated requirement (L3-113) of 150 hours per month.

10.3 Reliability Maintainability and Availability Requirements Compliance

Req ID	Requirement	Description	Design Compliance
L3-111	SPS Inherent Availability	SPS shall have an Inherent Availability (Ai) of at least 99.99 % while operationally capable.	Section 11.2.8 provides the LFAA.SPS Ai model and shows the calculated Ai to be ~100% given that the LFAA.SPS needs to remain Operationally Capable (i.e. > 95% of signal processing capacity).
L3-113	SPS Maintenance Hours	SPS shall require less than 150 Direct Maintenance Hours (DMH) per month at the Organizational Level (O-Level). Note: DMH/month = MTTR x number of equipment repair actions per month at the O-Level.	See Section 11.2.13.
L3-115	SPS Software Maintenance Down Time	SPS shall have a Maintenance Down Time (MDT) of less than 1 hours per year for software repairs. Note: Software MDT is defined as the time per year that SPS is unavailable as result of SPS software defect repairs and software maintenance activities during the telescope operational phase. SPS software defect repairs and maintenance that don't require SPS down-time are excluded from MDT.	LFAA.SPS is designed to minimise the down time required for S/W updates: • Each 'update' includes only the time for the mechanics of installing and updating LFAA.SPS on-line/operational equipment but not any associated pre or post-update planning or verification time. • TPM LRU software *installation* is performed without interruption of LFAA.SPS operation by 'pushing out' software into LRUs' local non-volatile storage via the M&C networks; they are subsequently *updated* with the new software on LRU restart/reboot (Section 5.2.2.5**)**. It is assumed no more than two major update events per year will be required and each event will require less than one hour.
L3-117	SPS Off-line Fault Detection Performance	When commanded and the SPS Administrative Mode set to OFFLINE, SPSF built-in diagnostic self-test capability	A detailed analysis of LFAA.SPS fault detection performance is provided in the LFAA Logistics

		shall detect and report 99% of all critical sub-element failures. Note: A Critical Failure is a failure that would prevent SPS being "Operationally Capable".	Report [RD55] during the construction phase
L3-118	SPS On-line Fault Isolation Performance	When commanded and with the SPS Administrative Mode set to OFFLINE, SPS shall isolate 95% of all failures down to an LRU level. Note: The SPS maintainer functions as part of the fault isolation mechanism by removing and replacing suspect LRUs.	An analysis of LFAA.SPS fault isolation performance is provided in the LFAA Logistics Report [RD55] during the construction phase
L3-114	SPS Mean Time to Repair	SPS shall have a Mean Time to Repair (MTTR) of less than 1 hour at the organizational level (O-Level).	See Section 11.2.8.

Table 10-3 Reliability, Maintainability and Availability Requirements Compliance

11 Safety

The LFAA.SPS design considers the following categories of safety:
1. Personal safety – avoiding risk of physical injuries, including those associated with sight, hearing, and lifting. The applicable regulation is the Australian Occupational Health and Safety Act [RD68].
2. Electrical safety - avoiding risk of electrocution. The applicable regulation is the European Low Voltage Directive [RD46] and more specifically IEC 60950-1 - Information Technology Equipment - Safety: General Requirements [RD11].
3. Asset protection safety – self-protection, external entity failure, fire protection. The applicable regulation is also IEC 60950-1 - Information Technology Equipment - Safety: General Requirements [RD11]].
4. Environmental safety – disposal of electronic waste. The applicable regulations that are acceptable in Australia are the Restriction of Hazardous Substances Directive (RoHS 2) [RD9], and the Waste Electrical and Electronic Equipment Directive (WEEE) [RD10].

The following sections address each of these categories and demonstrate how LFAA.SPS is designed with these safety issues in mind and to be compliant with the requirements.
This overall approach is consistent with the SKA Project Safety Management Plan.

11.1 Hazard Analysis

The LFAA.SPS hazard analysis [RD70] identifies the main hazards to personnel and equipment and documents how these are mitigated. The LFAA Element Safety and Hazard Analysis Report [RD56] also covers selected safety topics in greater detail.

11.2 Personal Safety

During LFAA>SPS installation, verification, operation, and maintenance, Personal Protective Equipment (PPE) is used (such as earplugs and gloves), and safety procedures followed, to reduce possible risk to personnel.

11.2.1 Rack Tip-over

The following 2 scenarios show how LFAA.SPS equipment racks (these can weigh up to 600 kg) can cause human injury or death as well as damage to the equipment they contain:

1. Seismic forces cause equipment racks to become unstable and tip over.
2. Downward force is exerted on equipment pulled out and extended from the rack to get access for maintenance, causing the rack to become unstable and tip over.

The following methods are used to stabilise the racks to mitigate these risks:

- Ensure racks have a centre of gravity (CofG) of less than 50% in the height direction by placing heavier equipment in the lower rack spaces and perform loading analysis to verify.
- Add front and back stabilizing feet (if required) to increase rack front-to-back stability.

Warning labels are placed on the front of racks to indicate that only one equipment item (e.g. LRU) may be extended from the rack at any given time. This is to warn integrators and maintainers to mitigate the rack tipping hazard.

11.2.2 Over-Temperature and Fire

To prevent equipment damage and a possible fire hazard, in the case where LFA.SPS equipment is not provided with adequate cooling, equipment temperature will increase up to a pre-defined limit at which point the hardware will autonomously power-off, even if monitor and control systems have failed.

11.2.3 Weight

Any LFAA.SPS equipment item weighing more than 23 kg presents an increased risk of human physical injury due to lifting and moving. Any equipment exceeding 23 kg is fitted with clearly visible permanent "warning lifting hazard" signage.
Any LFAA.SPS equipment items that have a mass of more than 23 kg, but less than 40 kg, will be designed with carrying handles that allow for a two-person lift. Such equipment will have signage to indicate that 2 people are required to lift it. Currently there is no such equipment in LFAA.SPS.
The only LFAA.SPS equipment items having a mass of more than 40 kg are the cabinets (Section 5.4.5), which can be fitted with an integral lifting arrangement such as eye-bolts to allow lifting equipment to lift and move them.

11.2.4 Sharp Edges

LFAA.SPS is designed and manufactured such that it has no sharp edges on access openings and corners.

11.2.5 Laser Light

LFAA.SPS has many optical fibre links that transport infrared laser light. A risk of permanent eye damage exists if humans stare into an open end of such a live optical fibre connection.
Wherever possible, equipment uses automated shutters. Where required, equipment is fitted with applicable optical warning signage.

11.2.6 Fire Protection

LFAA.SPS rack equipment must comply with the IEC 60950-1 or equivalent safety standard. "Fire-rated" materials retard the ignition and spreading of fire and are used throughout.

11.2.7 Personal Protective Equipment

During LFAA.SPS installation, verification, operation, and maintenance, Personal Protective Equipment (PPE) is used (such as earplugs and gloves), and safety procedures followed, to reduce possible risk to personnel.

11.3 Electrical Safety

This section mainly describes LFAA.SPS electrical safety requirements, design, and operation. The LFAA.SPS is designed, installed, and certified in accordance with the Australian or equivalent regulations, codes, and standards.

11.3.1 Rack Electrical Design

LFAA.SPS racks use COTS power distribution units (PDUs) certified to national and international electrical safety standards. The PDUs are connected to CPF and RPF mains 3-phase AC power via a National and International Electrical Regulatory Authority approved plug and socket.
LFAA.SPS racks and LRU equipment is procured and installed to comply with AS/NZS 3000:2007. (The Wiring of Premises) [RD50], or equivalent.
Shock Hazard warning labels and signs are provided where humans are exposed to shock hazards on and inside the racks, although the LFAA.SPS design is such that no such hazards exist outside of standard AC plug and socket use. Any access to shock hazard areas are secured inside enclosures or access panels. Any possible spare openings on chassis or faceplates are fitted with covers or plugs.

11.3.2 LRU Design

COTS and the bespoke TPM LRU are procured and designed to meet the ITE safety standard, IEC 60950-1.

11.3.3 Earthing and Electrical Bonding Systems

Earthing and Electrical Bonding systems are installed on LFAA.SPS racks and LRUs are to:

1. Provide a discharge path for ESD-induced voltages.
2. Provide protection against electrical shock by triggering earth leakage protection and over current protection devices (e.g., fuses or circuit breakers) to isolate faulty equipment.
3. Prevent voltage displacement, which could lead to electric shocks.
4. Prevent electrical arcing and sparking that may cause a fire hazard.

LFAA.SPS earthing/grounding systems are in accordance with the Australian codes and standards.

11.4 Environmental Safety

This section deals with toxic substances - materials, liquids, and gases.

11.4.1 Hazardous Materials

LFAA.SPS consists of COTS and bespoke information technology type electrical and electronic equipment. Many LFAA.SPS LRUs contain lead (e.g. RoHS-compliant electronics components contain small amounts of lead and polychlorinated biphenyl).
The LFAA.SPS limits the use of hazardous materials and adheres to the Restriction of Hazardous Substances (RoHS) directive. Equipment containing hazardous materials indicated in the directive is labelled as hazardous waste and is marked with the lead/silver contamination symbol and per the Waste Electrical and Electronic Equipment (WEEE) Directive 2012/19/EU category “IT and telecommunications equipment” (or equivalent).
Unrepairable or throwaway equipment containing hazardous materials is marked with applicable symbols/markings. These items must be disposed of by placing them in containers dedicated for this purpose to be subsequently transported to waste recycling centres (i.e., collection facilities) or approved authorised treatment facilities in compliance with Australian environmental protection and waste disposal legislation as well as regional local authority requirements.

11.4.2 Gases

LFFA.SPS is designed to not use or emit any hazardous gases, and materials are selected on the basis that they have reduced potential of emitting poisonous fumes/gases during fires.

11.4.3 Liquids

LFAA.SPS is designed not to use or emit any hazardous liquids.

11.5 Asset Protection

This section describes how LFAA.SPS protects the integrity of its equipment. Equipment safety concerns relate to overheating, loss of communication with MCCS and power consumption surges.
Each bespoke SPS LRU is outfitted with integral temperature sensing; when temperature trip points are reached, alarms are generated, prompting MCCS to take action, which could be either commanding the LFAA.SPS management to power down the LRU (i.e. in the case of only 1 or a few LRUs overheating), or commanding it to enter the Low Power state in a controlled/staged manner (i.e. in the case of large portions of, or the entire Sub-element, overheating) to keep power draw changes within the required rates (L3-153).
LFAA.SPS will continually make available temperature information and flag alarms when approaching or in an over-temperature situation. It is the responsibility of external entities to poll the flags and respond by commanding the LFAA.SPS to shut down some or all the system. If an over-temperature situation arises and no action is taken to respond to the alarm flagging, each SPS LRU has integral "deadman" thermal overload protection that automatically shuts down the LRU when a hard-defined temperature limit (75 C TBC) is reached, independently and not relying on CPUs or intelligent control threads (L3-95). Power to the over-temperature LRU will remain off until commanded otherwise by MCCS (L3-192). If sub-rack management has failed as well, once the LRU cools down sufficiently, it automatically powers up and, if applicable attempts to boot, however, the boot process won't continue without establishing communication with the sub-rack management and will remain in a reduced-power state (typically ~1/2 its normal power level, see Section 9.3.1).

Deadman thermal tripping may vary in time across the LFAA.SPS system since each LRU operates at a slightly different temperature and deadman devices trip at slightly different temperatures.

If the LFAA.SPS management is still operational in this situation, it flags warnings of a possible hazard (L3-186) since there is no way to *absolutely guarantee* that power draw changes are within required rates (L3-153). However, this situation should rarely, if ever, be encountered, and the disparities noted above should statistically guarantee power draw change limits.

Other COTS LRUs (switches) rely on built-in manufacturer's thermal overload protection for self-protection/fail-safe operation. Since none of these items are high-power units, no asset hazard is envisioned, and these are shut down in an orderly manner using rack PDUs as described at the beginning of this section (see Figure 6-9 for the location of all rack PDUs).

Power surges (i.e. voltage spikes) are suppressed by the LFAA.SPS PDUs and LRU power supplies with integrated transient suppression devices.

LFAA.SPS rack tip-over condition is alleviated by ensuring that racks have a low centre of gravity (< 50%).

11.6 Certification

The Occupational Health and Safety (OHS), Electromagnetic Compatibility (EMC), and Electrical Safety standards in Australia and Europe are not identical. To ensure that LFAA.SPS equipment certification is internationally acceptable, all equipment is certified by certification bodies that are members of the "Scheme of the IECEE for Mutual Recognition of Test Certificates for Electrical Equipment" or shortened to “CB scheme”.
“CB scheme” members can EMC- and safety-qualify equipment and issue CB certificates that are accepted by global National Certification bodies to speed up and simplify the approval and acceptance of equipment between countries.

11.7 Safety Requirements Compliance

Req ID	Requirement	Description	Design Compliance
L3-168	SPS Safety Legislation and Regulations	The LFAA.SPS equipment and operations shall comply with all applicable Australian Occupational Health and Safety legislation and regulations in accordance with the latest approved version of the LFAA.SPS to INFRA ICD.	LFAA.SPS equipment is IEC 60950-1 (Safety) compliant. **Electrical:** (see Section 12.3) LFAA.SPS design has no exposed hazardous voltages. LFAA.SPS racks have PDUs that provide equipment overcurrent protection. LFAA.SPS equipment has basic voltage surge protection. LFAA.SPS has basic fault current interrupt capability. LFAA.SPS equipment is connected to protective/safety earth. LFAA.SPS equipment is labelled to indicate electric shock hazards. LFAA.SPS equipment is designed, constructed, and installed to Australian regulations and standards (or equivalent). LFAA.SPS equipment chassis and racks are connected to safety earth. LFAA.SPS racks can manage the fault currents present at the power connection point. **Fire:** LFAA.SPS rack design uses non-flammable materials, components that won’t ignite a fire, and has no combustible materials.

			Mechanical: (see section 12.2) LFAA.SPS racks in same row are tied together to provide stability in sideways direction. LFAA.SPS racks have a Centre of Gravity (CofG) < 45% of the rack height. LFAA.SPS weight warnings are provided. LFAA.SPS lifting features are provided. LFAA.SPS rack design is sufficiently stable and will not have any sharp edges and corners. **Sound:** (see Section 12.2.3) LFAA.SPS rack audible noise levels limited < 85 dBA at a distance of 1 m.
L3-169	SPS Safety Certification	SPS rack and LRU equipment shall be safety certified to AS/NZS 60950.11:2015 or equivalent in accordance with the latest approved version of the LFAA to INFRA ICD.	This 60950.11 standard is a country-specific standard applicable to ITE equipment. The equipment will be compliant with the IEC version and the AS/NZS version. The AS/NZS version is almost identical to the IEC version with some deviations such as local electrical voltage, electrical connection types, ground/earth connection, etc..
L3-63	SPS Environmental Protection Regulations	The LFAA.SPS shall be compliant with all Australian state and national environmental protection legislation and regulations.	LFAA.SPS equipment is RoHS 2 directive compliant. See L3-210. LFAA.SPS equipment is Waste Electrical and Electronic Equipment (WEEE) Directive 2012/19/EU category “IT and telecommunications equipment” (or equivalent) compliant. See L3-103.
L3-210	LFAA.SPS Environmental Certification	The LFAA.SPS rack and LRU equipment shall be RoHS 2 (2011/65/EU)	LFAA.SPS equipment is RoHS 2 directive compliant. The equipment materials list

		certified in accordance with the latest approved version of the LFAA to INFRA ICD.	(BOM) is audited to confirm that it conforms to the directive. See Section 12.4.1.
L3-103	SPS Recycling and Decomposition	SPS equipment shall be compliant with environmental, ecological, safety, political and social legislation with regard to recycling and decomposition.	LFAA.SPS equipment is RoHS 2 directive compliant. SPS equipment is Waste Electrical and Electronic Equipment (WEEE) Directive 2012/19/EU category “IT and telecommunications equipment” (or equivalent) compliant.
L3-104	SPS Disposable Equipment Labelling	SPS disposable equipment shall be labelled as such.	LFAA.SPS equipment is Waste Electrical and Electronic Equipment (WEEE) Directive 2012/19/EU category “IT and telecommunications equipment” (or equivalent) compliant. Electronic Equipment is labelled to indicate how it needs to be disposed of or recycled.
L3-105	SPS Restriction of Hazardous Substances	SPS shall be compliant with the RoHS Directive 2011/65/EU (RoHS 2) or equivalent.	LFAA.SPS equipment is RoHS 2 directive compliant. See Section 12.4.1. (overlap of L3-210)
L3-170	SPS rack side-to-side stability	The LFAA.SPS racks shall be attached to adjacent racks in the same row to provide lateral stability in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS racks are attached to each other in the lateral direction to support individual racks. This prevents the racks from tipping over in case of seismic events and when heavy LRUs that are extended from the rack for maintenance.
L3-211	SPS Rack Acoustic Noise Level	The LFAA SPS rack acoustic noise levels shall be less than 85 dB (A) at a distance of 1 m or less from the rack in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS equipment is designed with fans that ensure a safe noise level is maintained at any rack location. See Section 12.3.2.

L3-172	SPS Equipment Shutdown on Failure	The LFAA.SPS shall autonomously detect and shut-down affected equipment in accordance with the latest approved version of the LFAA to INFRA ICD, when any of the following conditions occur: • an overcurrent condition occurs in a rack; • an over-temperature condition occurs in an LRU.	LFAA.SPS PDU equipment provides overcurrent protection. LFAA.SPS equipment LRUs individually have thermal shutdown protection (see Section 12.5).
L3-73	SPS Occupational Health Regulations	LFAA.SPS shall comply with all local Occupational Health and Safety legislation and regulations applicable to the Australian observatory site and its operations.	See L3-168.
L3-65	SPS Hazard Elimination	The LFAA.SPS shall not present a hazard to the operators, maintainers and own equipment with categorization exceeding the acceptable levels defined in the SKA Project Safety Management Plan [SKA-TEL-SKO-0000740].	See L3-168.
L3-68	SPS Fail Safe Operation	SPS equipment shall operate in a locally fail-safe manner and not rely on external safety devices or measures to operate safely.	LFAA.SPS PDU equipment provides overcurrent protection. LFAA.SPS equipment individually has thermal shutdown protection (see Section 12.5).
L3-47	SPS Fail Safe Provisions	The LFAA.SPS shall be safe from hazards in Categories I or II (ISO 45001) following an unplanned loss of main electrical power or main control functions.	LFAA.SPS equipment is IEC 60950-1 (Safety) compliant. See L3-1672. When LFAA.SPS rack power is restored, rack equipment powers back on and transitions to a safe state.

L3-69	SPS Non-Propagation of Failures	LFAA.SPS equipment hardware failures and software errors shall be safe from creating hazardous conditions in interfacing elements and sub-elements.	LFAA.SPS does not control any external equipment. External interfaces are defined to allow interfacing systems to operate autonomously and have self-protection
L3-48	SPS Fail-Safe State	LFAA.SPS equipment that would otherwise present a safety hazard when subjected to an unplanned loss of main electrical power or main control function, shall enter a designated fail-safe state.	LFAA.SPS equipment is IEC 60950-1 (Safety) compliant. See L3-48. When LFAA.SPS rack power is restored, rack equipment powers back on and transitions to a safe state.
L3-93	SPS Electrical Installation	The electrical wiring of all LFAA.SPS hardware shall comply with low voltage installation Standards (wiring of premises) AS/NZS 3000:2007.	LFAA.SPS equipment and racks are designed to comply and be installed in compliance to Australian standards.
L3-94	SPS Electrical Circuit Interlock	The LFAA.SPS shall provide electrical circuit inter-locks to prevent personnel coming into contact with hazards that cannot otherwise be eliminated from design.	LFAA.SPS equipment does not present any hazards that require electrical circuit inter-locks.
L3-96	SPS Safety of Equipment	The LFAA.SPS racks and equipment shall comply with IEC 60950-1 Information Technology Equipment - Safety Part 1 General Requirements or equivalent standard.	LFAA.SPS equipment is designed to comply with IEC 60950-1 Information Technology Equipment - Safety Part 1 General Requirements or equivalent standard. COTS equipment carrying this certification is selected; bespoke LRUs are designed to comply and could be certified. See L3-168
L3-97	SPS Power Interruption Survivability	LFAA.SPS racks shall survive a main power interruption at any time, without requiring a repair activity to restore	LFAA.SPS is designed to comply. See Section 5.4.1 for the behaviour of the TPMs in the event of a power failure.

		it once power is restored.	
L3-98	SPS Electrostatic Warning Marking	LFAA.SPS LRU equipment with electrostatic sensitive components shall be fitted with ESD warning labels.	LFAA.SPS is designed to not expose equipment internals to electrostatic shocks – see Section 5.4.1. Bespoke LRUs are fitted with appropriate ESD warning labels since opening it is an ESD hazard to internal electronics.
L3-99	SPS Equipment Identification and Safety Markings	LFAA.SPS equipment shall in accordance with ISO 61310_2 or equivalent bear all markings necessary: • for its unambiguous identification; • for its safe use; and supplementary information given, as appropriate: • permanently on the machinery; • in accompanying documents such as instruction handbooks; • on the packaging.	LFAA.SPS equipment is procured (COTS), developed, and manufactured in accordance with ISO 61310_2 or equivalent and bears all markings necessary.
L3-101	SPS Hazard Warning Marking	LFAA.SPS equipment that presents a potential hazard shall display a label in accordance with ISO 7010 or equivalent.	LFAA.SPS equipment that presents a potential hazard (e.g. shock, burn, sharp edge) displays a label in accordance with ISO 7010 or equivalent.
L3-102	SPS Label Robustness	LFAA.SPS labels shall be affixed for at least 50 years or the lifetime of the equipment, whichever is the smaller, and unlikely to come off during maintenance or as a result of the environment.	LFAA.SPS equipment uses durable labels that have a warrantee to stay affixed for at least 50 years, or the lifetime of the equipment.

12 Environmental

The LFAA SPS is located on-site and is distributed between the Central Processing Facility (CPF) shielded room and 36 Remote Processing Facilities (RPF) associated with Field Node clusters on the spiral arms of the Low Telescope in Australia. This section describes the environmental conditions the LFAA.SPS equipment is exposed to during transportation, normal operations and when in storage in the spare's storage facility

12.1 Transportation of Equipment

Commercial land, sea, and air transportation methods are employed to transport LFAA.SPS equipment to the CPF and RPFs during the integration, installation, and operational phases of SKA1_Low. These methods of transportation expose the equipment to various environmental conditions. The equipment must be sufficiently robust and be packaged to endure these transportation conditions with a high degree of confidence.

The equipment is designed to endure the transportation conditions and is qualified to the environmental limits specified in the ETSI / EN 300 019-1-2 ("Classification of environmental conditions; Transportation - Class 2.2: Careful transportation") [RD21] or equivalent standards (e.g., IEC 60721-3-2, [RD19]) (L3-135). The standard specifies the environmental condition limits that equipment is exposed to during transportation.

LFAA.SPS equipment is separately packaged at the LRU level, installation cable set, and bare rack and sub-rack level for transportation.

12.2 Storage of Equipment

LFAA.SPS equipment spares are stored at the spares store facility and need to endure the environmental conditions specified in ETSI / EN 300 019-1-1 (Part 1-1: Classification of environmental conditions; Storage, Class 1.1: Weather protected, partly temperature-controlled storage locations) [RD21] or equivalent standard (e.g., IEC 60721-3-1, [RD18]) (L3-135). The standards specify the worst-case environmental conditions equipment is exposed to during storage.

12.3 Operation

LFAA.SPS equipment is installed and used operationally in the CPF and RPF environments which are equivalent. LFAA.SPS bespoke equipment is qualified against the limits specified in the INFRA LFAA ICD [AD35] and indicated below.

LFAA.SPS COTS equipment is qualified to ETSI / EN 300 019-1-3 (Part 1-3: Classification of environmental conditions; Stationary use at weather protected locations) [RD23] or equivalent standard (e.g., IEC 60721-3-3, [RD18]) (L3-136).

12.3.1 Mechanical Environment

LFAA.SPS rack equipment may be exposed to the following mechanical vibration in event of a seismic event: a maximum peak ground acceleration of 1 m/s^2 [AD35] (L3-137).

12.3.2 Nominal Environmental Conditions

LFAA.SPS rack equipment is exposed to the following environmental conditions (L3-136):

1. Temperature range of cold air in front of racks: TBD °C to TBD °C.
2. Humidity Range: 5.5°C (DP) to 60% Relative Humidity (RH) and 15 °C DP TBC

3. Maximum Dew Point: ≤ 17 °C TBC
4. Maximum Temperature Rate of Change ≤ 5°C per hour TBC
5. Maximum Humidity Rate of Change Range ≤ 5% RH per hour, no condensation TBC

12.3.3 EMC Environment

LFAA.SPS equipment electromagnetically affects its own and other equipment via emissions and can be affected by its own and other equipment in the CPF (susceptibility). The EMC Control Plan (EMCCP) [AD25] documents the LFAA.SPS EMC campaign.

12.3.4 Susceptibility to Emissions

LFAA.SPS equipment is electromagnetically affected by its own and other Sub-element equipment located in the CPF and RPFs that are connected to the same electrical network.

12.3.4.1 *Susceptibility to Radiated Emissions*

LFAA.SPS LRU equipment that may be susceptible to radiated emissions from other equipment that is co-located in the CPF or RPF and is qualified to the IEC 61000-6-1/2 [RD33][RD34] or equivalent standard (specifically CISPR 24/35 [RD39][RD41] Class A) for immunity to radiated emissions as per the EMCCP [AD25].

12.3.4.2 *Susceptibility to Conducted Emissions*

LFAA.SPS equipment that connects to the CPF or RPF electrical networks is qualified to the following immunity standards or equivalent (specifically CISPR 24 [RD39] or EN 55024 [RD49] with performance criteria, for conducted emissions, to not require operator intervention to continue, as per the EMCCP [AD25]:

1. IEC/EN 61000-4-2 [RD26]: Immunity to ESD.
2. IEC/EN 61000-4-3 [RD27]: Immunity to Electromagnetic Fields.
3. IEC/EN 61000-4-4 [RD28]: Immunity to electrical fast transients/bursts.
4. IEC/EN 61000-4-5 [RD29]: Immunity to voltage surges.
5. IEC/EN 61000-4-6 [RD30]: Immunity to conducted disturbances, induced by RF fields.
6. IEC/EN 61000-4-11 [RD32]: Immunity to voltage dips, short interruptions and voltage variations.

12.3.5 Emissions

LFAA.SPS equipment will electromagnetically affect LFAA.SPS and other sub-system equipment in the vicinity, located in the CPF or same RPF that is connected to the same electrical network.

12.3.5.1 *Radiated Emissions*

LFAA.SPS LRUs are certified to the IEC 61000-6-3/4 [RD35][RD36] standard or equivalent (specifically CISPR 22/32 [RD38][RD40] or EN 55022 [RD37]) for radiated emissions.
In the worst case, emissions from LFAA.SPS equipment constructively sum and increase the maximum emission levels above that of a single emitter by a factor of N, calculated as follows:
Radiated emissions level increase = 10 x log10 (N)
The following table lists the equipment type, emission level, and number of the LFAA.SPS radiated emissions sources (L3-160):

Emitter Description	Certification	Count
SPS Cabinet	Class A	148
SPS Subrack	Class A	592
SPS Data Switches	Class A	296
Cabinet Management Board	Class A	148
Cabinet Fans	Class A	592
Cooling Circuit Pumps	Class A	592
Cooling Sensors	Class A	1480
Remote GPIO controller	Class A	148
Cabinet PDU	Class A	296
Total SPS Class A Emitters in the CPF		**4292**

Table 12-1 SPS EMI Emitters in the Central Processing Facility

Emitter Description	Certification	Count
SPS Subrack	Class A	12
SPS Data Switches	Class A	6
Cabinet Management Board	Class A	3
Cabinet Fans	Class A	12
Cabinet PDU	Class A	3
Total SPS Class A Emitters per RPF		**36**

Table 12-2 SPS EMI Emitters in Each Remote Processing Facility

The Data switches populated with transceivers are assumed to be compliant with CISPR 22 Class A. A switch with representational transceiver population will need to undergo EMC testing with representational data flows to confirm whether this is the case.

As a result, the LFAA.SPS equipment maximum radiated emission level is roughly 36 dB and 16 dB higher than the level for a single Class A device in the CPF and an RPF respectively.
A more realistic scenario is that emissions add randomly. In that case the radiated emissions level goes as the square root of the number of emitters, giving ~ 18 dB for 4292 emitters in the CPF and 8 dB for 36 emitters in each RPF.
The requirement for the number of electromagnet radiators (L3-160) is less than 4,500 for the CPF and 50 for the RPF. Consequently, the SPS is expected to be compliant.

12.3.5.2 *Conducted Emissions*

LFAA.SPS equipment that connects with the CPF and RPF electrical network is certified to the following emission standards (with performance criteria to not require operator intervention to continue):

1. IEC/EN 61000-3-2 [RD24]: Emissions of harmonic currents.
2. IEC/EN 61000-3-3 [RD25] Emissions of voltage changes, voltage fluctuations, and flicker.

In the worst case, harmonic current emissions from LFAA.SPS equipment constructively sum and increase the maximum emission levels above that of a single emitter by a factor of N for N emitters. Applying the same formula as above leads to the conclusion that in the worst case conducted emissions levels in the CPF are 42 dB above a single emitter. However, as above, the more realistic case is that emissions are ~21 dB above that of a single emitter. For the RPF these figures are 10db and 10dB respectively

12.4 Environmental Requirement Compliance

The following table provides required references to show requirements compliance

Req ID	Req Title	Req Text	Design Compliance
L3-147	SPS to INFRA Interface	The interface between SPS and Infra AUS shall be in compliance with the latest approved version of the SKA1 LFAA to INFRA Interface Control Document [100-000000-003]	The LFAA.SPS is designed to comply with these requirements with exceptions are noted, as per Section 13.
L3-148	SPS Deployment Location	SPS shall be located in the Central Processing Facility and Remote Processing Facilities in accordance with the latest approved version of the LFAA to INFRA ICD [100-000000-003]	LFAA.SPS is designed to match what the CPF and RPFs provide. This includes aspects such as rack space, power and cooling. See the start of Section 13.
L3-149	SPS Power Quality	SPS shall operate in compliance with the SKA1 Power Quality Standard Specification [SKA-TEL-SKO-00000293] in accordance with the latest approved version of the LFAA to INFRA Interface Control Document [100-000000-003].	LFAA.SPS equipment meets industry power quality standards (see Sections 13.3.5.2 and 13.3.6.2). Details of specific power quality conformance is provided in the requirements below (L3-151 to L3-167).
L3-151	SPS Power Factor	SPS rack equipment shall have a power factor in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment meet EMC emissions standard IEC 61000-3-2 [RD24] “Harmonic Current Emissions” Class D or equivalent. COTS equipment complies (see datasheets). The COTS and bespoke LRUs meet the Power Factor specification as per the PQ specification.
L3-158	SPS Harmonic Current Emissions	SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-3-2 standard or equivalent for Harmonic Current Emissions under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment meet IEC 61000-3-2 [RD24] Class A or equivalent standard for Harmonic Current Emissions. See the SPS LRU power supply specification [RD71].

L3-159	SPS Voltage Fluctuations and Flicker Emissions	SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-3-3 standard or equivalent for Voltage Fluctuations and Flicker Emissions under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment meet IEC 61000-3-3 [RD25] Class A or equivalent standard for Voltage Fluctuations and Flicker Emissions. See the SPS power supply specification [RD71].
L3-161	SPS ESD Immunity	SPS equipment susceptible to ESD shall be compliant with the IEC 61000-4-2 standard or equivalent standard for ESD immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment meet the IEC 61000-4-2 [RD26] Level 1 (4 kV contact, 8 kV air) Performance Criteria (A, B or C) or equivalent standard for ESD immunity or equivalent as defined in this section. See Section 5.4.1, the TPM design specification [RD71], and the SPS power supply specification [RD71].
L3-162	SPS Radiated, Radio Frequency, Electromagnetic Field Immunity	SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-3 standard or equivalent for radiated, radio-frequency, electromagnetic field immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment power supplies meet IEC 61000-4-3 [RD27] standard Test Level 2 (3 V/m) Performance Criteria (A or B) or equivalent for radiated, radio-frequency, and electromagnetic field immunity as defined in this section. See the SPS power supply specification [RD71].
L3-163	SPS Electrical Fast Transient/ Burst Immunity	SPS equipment connected to the CPF electrical network shall be compliant with the IEC 61000-4-4 standard or equivalent for electrical fast transient/burst immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment power supplies meet IEC 61000-4-4 [RD28] standard Level 3 (1 kV AC power line) with given Performance Criteria (A or B) or equivalent for Electrical Fast Transient/Burst immunity as defined in this section. See the SPS power supply specification [RD71].
L3-164	SPS Surge Immunity	SPS equipment connected to the CPF and RPF electrical network shall be compliant	LFAA.SPS COTS and bespoke equipment power supplies meet IEC 61000-4-5 [RD29]

		with the IEC 61000-4-5 standard or equivalent for Surge immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	Class 3 (1kV L-L, 2kV L-E on AC power, 1.5 kV L-E 10/700 u sec on signal lines) with given Performance Criteria (A or B) or equivalent standard for Surge Immunity as defined in this section. See the SPS power supply specification [RD71].
L3-165	SPS Immunity to Conducted Disturbances Induced by Radio Frequency Fields	SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-6 standard or equivalent for immunity to conducted disturbances, induced by radio-frequency fields under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment power supplies meet IEC 61000-4-6 [RD30] Level 2 (3 V rms on power and signal lines) with given Performance Criteria (A or B) or equivalent standard for Immunity to conducted disturbances, induced by radio-frequency fields as defined in this section. See the SPS power supply specification [RD71].
L3-166	SPS Power Frequency Magnetic Field Immunity	SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-8 standard or equivalent for power frequency magnetic field immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment power supplies meet IEC 61000-4-11 [RD32] (for equipment requiring <16 A, else EN 61000-4-34 for equipment requiring >16A) Class 2 (0% input Voltage for 10 ms, 70% for 500 ms) with given Performance Criteria (A or B) or equivalent as defined in this section. See the SPS LRU power supply specification [RD71].
L3-167	SPS Voltage Dips, Short Interruptions and Voltage Variations Immunity	SPS LRU equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-11 standard or equivalent for voltage dips, short interruptions and voltage variations immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.	LFAA.SPS COTS and bespoke equipment power supplies meet IEC 61000-4-11 [RD32] (for equipment requiring <16 A, else EN 61000-4-34 for equipment requiring >16A) Class 2 (0% input Voltage for 10 ms, 70% for 500 ms) with given Performance Criteria (A or B) or equivalent as defined in this section. See the SPS LRU power supply specification [RD71].

L3-106	SPS EMI and EMC	SPS equipment shall be compliant with the emission and immunity standards in the SKA EMI/EMC Standards and Procedures [SKA-TEL-SKO-0000202] document.	In accordance with EMCCP [AD25], LFAA.SPS COTS equipment is CISPR 22/32 [RD38]/[RD40] Class A compliant. Bespoke equipment is at least CISPR 22/32 Class A compliant – see Section 5.4.2. Also see the SPS power supply specification [RD71].
L3-107	SPS Essential Conducted and Radiated Electromagnetic Emissions	SPS LRU equipment that radiate electromagnetic emissions in the SKA1 frequency range and that aren't within a shielded enclosure of a higher level LRU, shall at a minimum be compliant with the IEC 61000-6-4 standard or equivalent for conducted and radiated emissions under standard test conditions and setups in the SKA Low telescope frequency range as specified in the SKA EMI/EMC Standards and Procedures [SKA-TEL-SKO-0000202].	LFAA.SPS COTS equipment is at least CISPR 22/32 [RD40]/[RD40] Class A compliant. Bespoke equipment is certified to at least CISPR 22/32 Class A – see Section 5.4.2. Wherever possible, COTS equipment is selected that is CISPR 22/32 Class B compliant and the SPS bespoke LRUs are designed with the goal of meeting Class A (L3-160).
L3-108	SPS Electromagnetic Susceptibility	SPS equipment shall be compliant with the IEC 61000-6-2 standard or equivalent for susceptibility to conducted and radiated emissions under standard test conditions and setups. Note: Only LRUs with electrical or electronic components that are susceptible to EMI and that aren't within a shielded enclosure of a higher level LRU need to be checked for compliance.	LFAA.SPS COTS equipment is at least CISPR 22/32 [RD38]/[RD40] Class A compliant. Bespoke equipment is certified to at least CISPR 24/35 [RD39]/[RD41] Class A.
L3-109	SPS Essential Off-the Shelf Equipment EMC marking	SPS "off-the-shelf" LRU equipment shall as a minimum be CISPR 22 and 24 Class A or equivalent compliant over the SKA telescope frequency range.	LFAA.SPS COTS equipment is at least CISPR 22/32 [RD38]/[RD40] and 24/35 [RD39]/[RD41] Class A compliant. Selected COTS equipment is Class A compliant (L3-160).

L3-110	SPS Electricity Network Electromagnetic Compatibility	SPS equipment shall follow the code of practice for the application of Electromagnetic Compatibility (EMC) standards and guidelines in electricity utility networks.	See previous EMC detailed requirements above for compliance. See L3-106 to L3-109.
L3-134	SPS Storage Environment	SPS equipment, while in its storage packaging, shall withstand, and shall operate to specification as defined herein after exposure to, the storage environmental conditions as defined in “Class 1.1: Weather protected, partly temperature-controlled storage locations” of the ETSI EN 300 019-1-1 standard and defined in BS EN IEC 60721-3-1. 1. Climatic Conditions 1K3 2. Biological Conditions 1B2 3. Chemical conditions 1C2 4. Dust and Sand conditions 1S2 5. Shock & Vibration Conditions 1M2	LFAA.SPS COTS equipment is selected to be compliant with the storage environment or equivalent. Bespoke equipment is qualified to the same environment.
L3-135	SPS Transportation Environment	All components and spares of the SPS, in their transport packaging, shall be safe from damage while, and shall perform to specification as defined herein, after being transported under conditions as defined in "Class 2.2: careful transportation" of the ETSI EN 300 019-1-2 standard [37] and defined in BS EN IEC 60721-3-2: - Climatic conditions 2K5H - Biological conditions 2B3 - Chemical conditions 2C1 - Dust and Sand conditions 2S3 - Shock & Vibration conditions 2M3	LFAA.SPS COTS equipment is selected to be compliant with this transportation environment or equivalent. Bespoke equipment is qualified to the same environment.

L3-136	SPS COTS Operating Environment	The SPS "off-the-shelf" equipment shall perform to specification as defined herein during operation under the environmental conditions as defined in the ETSI EN 300 019-1-3 standard for "Class 3.6: Telecommunication control room locations" or equivalent.	LFAA.SPS COTS equipment is selected to be compliant with this operating environment. Bespoke equipment is qualified to the same environment.

Table 12-3 Environmental Requirements Compliance

13 Development Support

The LFAA. SPS design requires the development of bespoke hardware, software and FPGA code components. To support the developments there are several key facilities or environments required:

- LFAA.SPS Integrated Test Facility (ITF)
- Emulators for LFAA.SPS verification
- FPGA code development framework
- FPGA code compilation tools
- Software development environment
- Code regression testing system
- LRU Automated Test Environment (ATE)
- Temperature chamber test facility
- Failure reporting database and analysis
- EMI certification facility

These environments will allow LFAA.SPS to progress through development as well as the acceptance testing detailed in RD2. It will be supported by appropriate management and system engineering activities such that development can occur unimpeded. A majority of the developed support facilities will likely become part of the SKA operations following the completion of the construction phase. Each of the support items are detailed further in the following subsections.

13.1 LFAA.SPS ITF

The components that comprise the LFAA.SPS Sub-element will be integrated and tested at a test facility known as the LFAA.SPSITF. The test facility provides a typical data centre environment, similar to the SKA Low Central Processing Facility (CPF) building. The location of the LFAA.SPS ITF shall be at the design headquarters for reasons of efficiency (e.g., at INAF). This would be staffed by an on-site test engineer who installs and maintains the equipment.

The AIV roll-out plan (AD20) expects a “stable and well-tested” Sub-element to be available at the LFAA.SPSITF for informal testing before the initial qualification event. Testing at the LFAA.SPSITF continues throughout the engineering construction period until AIV handover to SKA1 operations.

As detailed in Section 16 there is always one rack of equipment containing a representative system at the LFAA.SPSITF. This rack will require supporting infrastructure that includes the following items:

- 3-phase power (up to 10 kW) with earth leakage breakers
- Liquid chiller, pump and filter (in excess of 10kW capacity)
- Optical networking interfaces for development engineers
- Appropriate building sensors and alarms (fire, liquid leakage, security, etc.)
- Air conditioning to maintain similar temperature/humidity as at the CPF
- In addition to the infrastructure facilities there are several other ITF items which shall be available to support the developments:
- Liquid cooling – flushing, air purge and priming equipment
- Liquid cooling gauges (flow, temperature) and clear inspection hose
- Ethernet traffic generator and analyser with 10, 25, 40 and 100Gbps interfaces
- Reference clock and PPS generator
- Fibre optics ribbon and individual fibre cleaning and inspection station
- Fibre optics power meter
- Computer, keyboard, mouse and monitors external to the rack that show system configuration,
- health and execute local testing

- LFAA.SPS must be tested for conformance with level 3 requirements
- These verification requirements can be grouped according to LFAA.SPS functionality included
- for the initial AIV qualification event and subsequent array releases. The verification activity is performed at the LFAA.SPS ITF using the user interfaces described in Section 5.3.4.

13.2 Emulators

LFAA SPS includes an external element interface with CSP for delivering beam products and associated meta-data. There are also LFAA internal Sub-element interfaces with FN and the MCCS. LFAA.SPS is expected to perform standalone verification of these interfaces prior to Sub-element integration at the AIV System ITF. This will be completed prior to the initial qualification event giving time to perform some integration verification of the internal interfaces at the CSP ITF.
Standalone verification testing involves inspection and measurement of the interface's properties and functional capabilities. This includes exercising the interface using test equipment to emulate the missing party. Standalone verification is discussed for each individual interface in the following subsections.

13.2.1 Field Node Emulator

The Field Node to SPS interface 5.3.5 uses standard Ethernet for the Field Node Control and Monitoring physical interface and RF over Fibre for the dual polarisation Field Node signal for each antenna.
Emulation of the Control and Monitoring interface is easily achieved with a Computer or server running software scripts emulating an APIU management node.

13.2.2 MCCS Emulator

LFAA.SPS interface verification can be performed by running MCCS and LFAA.SPS M&C software together on a single server. This is expected to be performed as part of the SKA continual integration testing process introduced in [AD28].

13.2.3 CSP Emulator

The verification of the LFAA.SPS interface to CSP can be performed using a CSP Emulator. This would provide the capability of capturing data buy hosting 100 Gbit/s on one or more servers. This is expected to be performed as part of the SKA continual integration testing process introduced in

13.3 Code Regression Testing

The development plan includes the development of unit tests and test benches for execution within a continuous integration testing environment. This is expected to be a simulation environment for FPGA firmware and the execution of test scripts for system-level tests (software/ hardware). As new functionality in software and FPGA is introduced during construction there is a need to perform regression testing at two levels:

1. Functional testing: simulation of FPGA signal processing and the Matlab model
2. Behavioural testing: real-time analysis of the software and FPGA signal processing

Regression testing of the functional units is a time-consuming exercise as this operates in a non-real-time environment. In a real-time environment these occur much faster and may also involve the use of emulators to provide greater test coverage when required. It is important to exercise all available modes of operation at both levels of testing. The captured results, either simulated, FPGA or

emulator captured, will require analysis to determine functionality and performance. Hooks will be placed in both FPGA and software code to facilitate such testing as this will reduce the time to develop and verify system compliance. Tests will be executed at

- Regular intervals (e.g., every month)
- After checking in new code
- During verification events (e.g., AA1)

Having an automated verification system to support the development will increase compliance, test coverage and reduce the time needed to verify the system.

13.4 ATE

The SPS LRU will be produced in reasonably large quantities which, given the number of components per LRU, would benefit from the use of Automatic Test Equipment (ATE) to perform measurements and evaluate the test results. The ATE is a system containing test instruments as well as a server executing customised test software.

During the operation of the LFAA.SPS system it is expected that faults will develop due to the ageing of the equipment. An ATE will facilitate the quick diagnosis of LRU faults such that they can be repaired and returned to the working system. It is also considered good practice to test an LRU before it is placed into a working system after a long period in storage. An ATE provides this mechanism.

An ATE performs two functions: the first is to test whether the Device Under Test, DUT, is working correctly, and the second is when the DUT is not working correctly, to diagnose the fault. The ATE can reduce an LRU fault to a localised group of components. Designing the ATE requires knowledge of the system and its behaviour. It is important in the design stage of the LRUs to appreciate the testing that will be performed in the ATE. Two levels of ATE testing are required:

- Low-level PCBA connectivity testing using a JTAG interface
- High-level LRU functional testing using the M&C Ethernet interface

JTAG/Boundary scan can be implemented as a PCB-level or system-level interface bus for controlling the pins of an IC and facilitating continuity (interconnection) tests on the DUT. The ATE also runs a test script that controls the operation of the various test instruments in the test system, to coordinate a sequence of actions in the overall test. For the ATE the following pieces of additional equipment (with control interfaces) are required:

- DC power supply
- Mechanical support for the LRU (such as a sub-rack)
- Liquid chiller (including an air purging system)
- Optical cabling assembly
- Known working LRUs (“golden samples”)
- Multiple ATE-s will be built for testing at the following locations:
    - Manufacturing facility where the parts are assembled into LRUs
    - CPF (O-level, see Section 17) where LRUs are tested before installation into the working system
    - Repairs (I-level) where failed LRUs are restored to working order

13.5 Temperature Chamber

During construction the response of the LFAA.SPS supporting and processing subsystems to temperatures within the specified operating temperature range is checked. Such temperature environments could be created by the following means:

- Raise the operating temperature of each rack (turning off is also possible but will generate alarms)
- Place subsystems in a temperature-controlled chamber

Temperature changes within a rack will result in small deviations from normal operating temperatures and should not have an adverse effect on the overall system. However, in a temperature-controlled chamber the subsystems can be exercised well beyond normal operating conditions. Such temperatures will reveal system weaknesses under operating conditions as well as storage/transport conditions (i.e., they effectively force product weaknesses to emerge by accelerating fatigue). For example, the TPM could be placed in the temperature chamber and the ATE test scripts run continuously over a period and temperatures. The testing results as well as field failure and repair data (from ITF-QE to AA4) will:

- Indicate design and manufacturing deficiencies and can be used to provide quality and reliability trends
- Assist O- and I-level spares provisioning and maintenance schedules to be optimised
- Assist in rating the subcontractors' quality
- Contribute statistical records for future reliability and repair time predictions

13.6 Failure Reporting

In both the ITF environments and on the operational site formal failure reporting documentation or database is essential to ensure field data collection is sufficient and consistent.
The LFAA.SPS failure reporting document will contain key information:

- Date of failure
- Total operating time (recorded monthly)
- Failed hardware component and root cause
- FPGA/Software code failure and root cause

This will be reported monthly during construction by counting the number of failures in all types (hardware, software and FPGA code) per month, as well as an accumulative number of failures over time. This will further develop the operations model and design documentation during the construction phase.

13.6.1 EMI Certification

The LFAA.SPS processing consists of a custom LRUs and COTs items such as switches populated with transceivers which will require appropriate EMI certifications. It is not envisaged that LFAA.SPS would build such a test facility as part of its development but rather use an existing certified facility. Such services are offered by many vendors; however, one will be selected that can also accommodate the associated ATE setup. It is important that the SPS equipment is functioning as close to normal operations as possible. EMI certification should be used early in the design cycle such that design improvements can be made if required.

14 Production and Manufacturing

AAVS1 experience has been a very good bench test to understand several critical issues for a small production (only 400 antennas against 138.000 receptors for LFAA) from the manufacturing/production point of view. Of course, it should be exploit better for the future with the companies will drive the real production for SKA Low but, at the moment, the bigger risks we envisage are related to the most complex part that is the ADU board. In the next paragraphs we will describe the manufacturing process and the related risk analysis of the TPM ADU, based on the AAVS1 experience (revision 1.2.)

The TPM ADU board is a complex design that incorporates several critical issues with related risk. In the design phase, a preliminary risk assessment has been accomplished to apply suitable design techniques for risk mitigation and define testing strategies for manufacturing.
The following main issues has been considered:

- Design complexity: number of components on the board and procurement;
- Design density: component placement, power model and heat extraction;
- Design for manufacturing: pcb technology, product testability.

One of the objectives of the design, is manufacturability for a long period of time.

14.1.1 Analogue receiver Production & Manufacturing

The SKA LFAA Receiver - Front End and Pre ADU assemblies is a complex design that incorporates several critical issues with related risk. In the design phase a preliminary risk assessment has been done to apply mitigation technique by design and define the testing strategies for manufacturing.
The following main issues has been considered:

- design complexity: number of components on the board and procurement
- design density: component placement, power model and heat extraction
- design for manufacture: PCB technology, product testability

One of the objectives of the design, clear from the beginning, is the manufacturability for a long period of time

14.1.2 Design complexity

The Front End and Pe ADU assemblies involve about 100 different part numbers to implement all the required functions. The components have been classified by function and for each the following criteria have been applied for component selection:

1. One market leader (industrial/military) has been selected in each class, to partner with and build a long-lasting procurement relationship for all single source devices;
2. Each component has been chosen for the best performance, the production status and the production technology (only almost new production process has been selected)
3. Component uniformity for solderability has been verified (compatible pin pitch and component size/weight), considering automatic lead free SMT process as mandatory.

For point 1, the following classes have been identified: FPGAs (Xilinx, Lattice), memories (Micron), Analogue to digital components (Analogue Devices), DC-DC supplies (Texas Instruments), linear supplies (Analogue Devices), capacitor (Murata), inductors (Coilcraft) and connectors (Samtec).

Several single source devices have been selected to accomplish the requested performance, size and cost. The component availability shall be monitored to schedule board updates during the LFAA lifetime.
No component with pad pitch smaller than 0,5 mm has been chosen, to allow a Printed circuit board that provide a solder mask without missing.

14.1.3 Design density

The TPM – ADU component placement on the PCB has been done considering functional performance, heating and manufacturability. The board size is small with respect to the component densities; in consideration of that, the following design rules has been applied:

- All t main components have been placed on the TOP side, with some exceptions for ease of soldering process, heating extraction and the testing;
- No component is placed with vertical overlap;
- Component placement has been done to allow automatic 3D inspection;
- All supplies are accessible with a bottom placed test point, ready for a needle bed.

The design density and component size will not allow a “Flying probe” test. It is assumed that the board production testing will be done with the latest 3D optical inspection machines, electrical test and then functional test.

14.1.4 Design for manufacturing

The TPM – ADU design for manufacturing has considered the following items:

- Solderability process;
- PCB procurement;
- Assembled board testability.

For the solderability process, the component library shape has been verified with the soldering company to define the process. Pad solder apertures, thermal pad design and via in pad construction rules have been defined in accordance with the selected solder laminate thickness. The library tuning has been done between the first PCB revision 1.0 and the second one 1.1, capturing the production issues directly from the process.
The PCB is the only custom element involved in the TPM-ADU production process and the involved quality process shall be defined and monitored, with respect to the specialised companies that execute it.
PCB procurement is related to the technology chosen for its design, mainly:

- PCB material selection and stack up (number of layer and thickness);
- PCB intra-layer connections (vias);
- Trace minimum thickness and minimum insulations.

The TPM ADU PCB material, structure and layout rules have been defined in the feasibility study at the beginning of the process.
To meet the cost, a combination of two different dielectric materials has been chosen: a medium high-speed material for the outer layers (ISOLA FR408 HR) and a standard material for the inners (ISOLA FR4 HTG). This choice shall be considered as Manufacturing Risk for the PCB manufacturer, who should treat the process according to that.

The remaining PCB layout has been done avoiding PCB construction possible issues (e.g. traces larger than 3.6 th., insulation greater than 5 th for trace and 6 th for planes, no blind vias).
The PCB construction process is very complex, the adopted production process shall be defined, and the corresponding quality inspection process shall be fixed.
The last manufacturing process, after the board soldering is testing that shall guarantees the board functionality and quality Testing is accomplished at several layers:

- Optical & mechanical check;
- Electrical check;
- Functional check;
- Performance check, marginality analysis;
- Performance check, analogue acquisition quality.

The Optical & Mechanical check is done with the latest 3D optical inspection machines that can verify the conformance of each board to a sample with, at example the following checks:

- Presence of all components, check of the package code if present;
- Position of components, rotation, height and planarity;
- Presence of solder material on the pads.

The electrical check verifies the impedance of all board supplies and voltages of powered circuits.
The functional test verifies that all components can be programmed and provides access to their control interface.
In the performance check, all devices are programmed with a Functional Built In self-test application that performs the following:

- Verify that all interfaces between components work at nominal speed transferring test data (internal and external board interfaces);
- Measure, where possible, the quality of transmission in terms of “transmission valid windows”, that is mono-dimensional for the generic I/O interface and bi-dimensional for the transceivers;
- Provide diagnostic information in case of failures.

The objective of this test is to ensure that all devices are working at nominal speed and can transfer data among each other without errors. The quality test can also provide an indirect check for the production process quality, covering PCB manufacturing and soldering process.
The selection of valid acceptance criteria of the previous test defines rigid quality criteria that contribute to manage the manufacturing risk covering the following items:

- PCB defect, line impedance errors;
- Components defects, with focus on clock distribution;
- Supply defects, in terms of supply high frequency noise or ground noise.

Some aging process shall be introduced like thermal cycles and the test repeated on some samples for each production lot.
The last analogue performance check applies a set of high-quality monochromatic signals to each input and verifies the RF acquisition performance on the selected bandwidth. This procedure can verify the respect of the design margin for each RF input and diagnose common mode or single channel board defects, including clock distribution, supplies or single component defects. This test

eliminates the risk that a single channel of a TPM board does not respect the requested analogue performance.

14.1.5 Manufacturing risk table

- Assuming that the strategies and the activities described in the previous section has been adopted, almost the following risk shall be considered, related to humans' errors, design limits, commercial situation and other reasons not directly related with the design and testing process.

Risk description	***Causes***	***Expected effect***	***Mitigation***
Component procurement	Out of stock, obsolescence	Production stop	Component production status monitoring, supplier agreement, volume purchase, board redesign
Soldering process variations	Changes in the supplier process	Possible quality variations	Execute aging and marginality test
Procurement error	Mistake in the pick & place process	Functional or performance errors	Functional and marginal test
Soldering error	Lack of solder paste, incomplete reflow	Unperfect soldering, board accelerated aging	Define a quality process with the supplier: Complete check of the soldering process, accurate 3D optical inspection, execute lot aging test, execute on line marginality test
Component aging	Time, working temperature, correct point of load	Performance loss	Marginality analysis and design margin applied
High speed devices error budget [2]	Component performance marginality	Errors, functional loss	Verify marginality analysis test coverage, spare parts available
Component production change	Change in the component manufacture process	Functional variations	Procurement monitoring, impact analysis, complete test for the related production lot
PCB production process	Material and process changes	Performance change, PCB defects	Lot test, accelerated aging and test, quality inspections
Interface connectors	Bad contacts for dirty or oxidation	Signal transmission degradation	Contact protection, diagnostic tools

[2] Several high speed interface are used in the TPM design, it is possible that due to component production process differences functional errors appear randomly when the circuit operates at maximum performances.

15 Commissioning

The LFAA.SPS design and implementation phases will support the AIV Element roll-out plan [RD51]. Core to the AIV plan are the telescope-level commissioning phases shown in Table 15-1 where there are five key milestones, one ITF Qualification Event (ITF-QE) and four Array Assemblies (AA).

For the ITF-QE and AA1 an initial system supports 24 Stations which requires 12 complete SPS cabinets each populated with 4 sub-racks which in turn are each populated with 8 TPM LRUs. This is a total of 384 TPM LRUs. This system will generate all 384 coarse channels internally but will only forward a bandwidth of 75MHz with all channels having the same pointing.

Even though only basic functionality is implemented, the design incorporates much of the functions used in the final design with the notable exception of RFI flagging which occurs in AA2 through to AA4. A significant period is needed to establish these initial systems. Thereafter, shorter intervals are needed between releases with incremental steps in functionality. LFAA.SPS will align appropriate production and code release phases to the AIV release schedule.

	ITF-QE	Array Assembly 1	Array Assembly 2	Array Assembly 3	Array Assembly 4
Stations	24	24	64	256	512
Sub-arraying	-	1	16	16	16
Sub-stations	-	-	-	-	1024 and 2048
Bandwidth	75 MHz	75 MHz	150 MHz	300 MHz	300 MHz
Station Beams	1	8	8	8	8
RFI	-	-	Fixed flagging from TM	Simple power threshold flagging	Final RFI detection scheme

Table 15-1 Array Assembly events and LFAA.SPS functionality

There are four physical locations where hardware will be required:

- LFAA.SPS ITF – local to the sub-element where development and debugging can occur rapidly in a team environment. Element and sub-element emulators provide enough test and capture capabilities (defined by their ICDs) to sell off at level-3.
- LFAA Element ITF – where LFAA sub-elements integrate to test internal interfaces (e.g., SPS to MCCS) and functionality. Only element-level emulators are required to test and sell off the system at level-2. This will likely be the same facility and hardware as in the SPS ITF.
- AIV System ITF – where elements are verified (sold off) against requirements. Elements are integrated together to perform final verification at level-1. Sub-element warranty starts after the element sell-off acceptance test.
- Site CPF / RPF (Central and Remote Processing Facilities) integration of the hardware in its final location and tested with on-sky data. CSP are observers of the AIV verification testing.

15.1 Hardware Commissioning

The estimated minimum quantity of hardware and its location is shown in Table 15-2. It is assumed that the LFAA.SPS construction team will always have hardware local to their location such that development can occur independent of the array assembly events.
For AA2 an eighth of the system is installed comprising 32 cabinets, 128 sub-racks (1024 TPMs) configured for outputting a bandwidth of 150 MHz which may be allocated across up to eight

pointings. At AA3 half the full SPS hardware is installed with the full 300MHz output bandwidth but only at AA4 is the full SPS functionality implemented.
At the completion of the warranty period for the full system the LFAA.SPS construction team hardware is handed over and becomes part of the system spares. The hardware at the LFAA.SPS ITF will also be eventually used as spares.

AIV Assembly	CPF/ RPF (cabinets, sub-racks, TMPs)	AIV System ITF (cabinets, sub-racks, TMPs)	LFAA.SPS ITF (cabinets, sub-racks, TMPs)	Total (cabinets, sub-racks, TMPs)
ITF-QE	-	12, 48,384	12, 48, 384	24, 96, 768
AA1	12, 48, 384	12, 48,384	12, 48,384	36, 144, 2304
AA2	32,128, 1024	12, 48,384	12, 48,384	44, 176, 1408
AA3	128, 512, 4096	12, 48,384	12, 48,384	140, 560, 4480
AA4	256, 1024, 8192	12, 48,384	12, 48,384	268, 1072, 8576

Table 15-2 Hardware requirements for supporting and processing equipment for each array assembly

Critical to the commissioning of the production hardware are the emulators to verify the functionality of the system against system requirements. Pivotal to early testing is the development of emulators that produce or capture data that is equivalent to that of Sub-elements or elements that are designed by others. The emulators only contain partial functionality and are designed to test a portion of the system.
Once sell-off occurs at each array assembly the associated hardware is left alone (i.e., for exclusive AIV L1 and L2 commissioning use) until the new array assembly installation is ready for AIV. This leaves no gaps in the LFAA.SPS availability for the telescope commissioning teams. This requires two closely-aligned consecutive phases of on-site sell-off for each array assembly:

- Where possible new hardware is installed by LFAA without disruption to existing hardware (this is not always possible as there are connections between racks and external equipment which may cause temporary disruptions).
- The software and FPGA code configuration are updated, and the LFAA system verified, and sold-off. Since this hardware is identical (i.e., identical build versions or equivalent) to what was just installed, the verification effort should be greatly reduced and should mostly consist of newly-installed software and FPGA code configuration checks along with some operational spot-checks. The system is then accepted by AIV.

15.1.1 Production Readiness Reviews

A key part of the roll-out plan is a series of Production Readiness Reviews (PRR). PRRs are a necessary stage before procurement of hardware can commence. PRRs will occur for both supporting and processing equipment to ensure that hardware being purchased meets the requirements. For each piece of equipment at level-5 in the PBS there will be a corresponding PRR. The PRRs will be distributed over a period and not all occur at the same time. Once the PRRs are approved then volume production will commence. It is important for FPGA and software code developers to have a consistent and stable hardware platform.
LFAA.SPS will use Xilinx Ultrascale+ XCKU9P 16 nm FPGA devices. This will allow the LFAA.SPS to be constructed with mature technology. Experience has shown that next generation technology will not significantly lower cost. With the current construction timeline adoption of newer technology would increase risk.
In addition to the emulators the custom hardware will require an Automated Test Environment (ATE) to verify the performance of each LRU. This ATE will have supporting FPGA code to exercise the LRU capabilities in a controlled environment. The ATE will test the following items:

- Mechanical conformity
- M&C functionality
- Voltage regulation and power consumption
- Cooling systems
- Optical connectivity (speed and optical power)
- Memory performance
- PCBA connectivity check using JTAG
- Analogue signal chain performance including cross-talk and data conversion

15.2 Code Commissioning

There will be many releases of code internal to LFAA.SPS. Coding occurs in a pairwise manner such that the FPGA code is supported by corresponding management software. As new functionality is added to the FPGA the software keeps abreast with these developments to facilitate commissioning of the new FPGA functionality. As the functionality of the code increments and passes qualification testing the code release can be made. The version of the software must match a corresponding version of the FPGA code.
The order in which code is commissioned is dictated by the AIV roll-out plan. Within each release there will be several minor releases. Sufficient built-in test functions (generate and capture modules) will be incorporated into the FPGA code such that the management software can test the functionality of smaller groups of FPGA code. This will enable the commissioning of the LFAA.SPS with much finer granularity than the AIV schedule.
System health and hazard prevention is expected to be established early in the construction phase. User Interfaces (UIs) at multiple levels of system hierarchy are developed from the beginning with a use model for them that encompass engineering development and test, through to system commissioning and operational support/maintenance. For each code release there will be a corresponding user interface with appropriate functionality enabled to support the system. At the LFAA Element ITF this includes integration with the MCCS which is developed using the Scaled Agile Framework (SAFe). This will see quarterly software releases which are not synchronised to the array releases but instead will evolve over time. Once at the AIV ITF, the same will occur with integration of TM.

15.3 Verification and Acceptance

The LFAA.SPS is responsible for the verification of L3 Requirements. This requires the element to use emulators to simulate input data and evaluate output data. For many requirements the sell off at L3 is identical to the sell off at L2 for LFAA including non-functional requirements. The documentation of the L3 testing, as described in [AD43], will be supplied to AIV to demonstrate compliance. Requirements needing a specific verification at L2, in general those for MCCS and Field Node will have this testing done at the LFAA Element ITF. Again, these tests will be documented and supplied to AIV. L1 verification is conducted at the AIV ITF.
The hardware will undergo Factory Acceptance Tests (FAT) at the LFAA Element ITF in the presence of AIV. AIV signs off the FAT and then LFAA will transport the hardware to the AIV ITF or the CPF/ RPF site for installation and handover to AIV. For AA1 identical equipment is installed at the AIV ITF and the site. On site this is a temporary AA1 facility as the CPF is yet to be constructed. The AA2 SPS is installed in the new CPF/ RPF buildings and operate in parallel with the AA1 equipment. The ITF SPS equipment are reconfigured for AA2 verification.
When the AA1 SPS is no longer required it will be decommissioned and put into storage for reuse in the AA3 equipment.

16 Integrated Logistic Support

This section describes the SPS Logistic Support (ILS) approach. Many aspects addressed here are described in more detail in the LFAA Logistic Engineering Report [RD55]. OPEX detailed costing for SPS logistics is provided in [RD54].

16.1 Support and Maintenance Concept

The figure below shows the SPS maintenance concept:

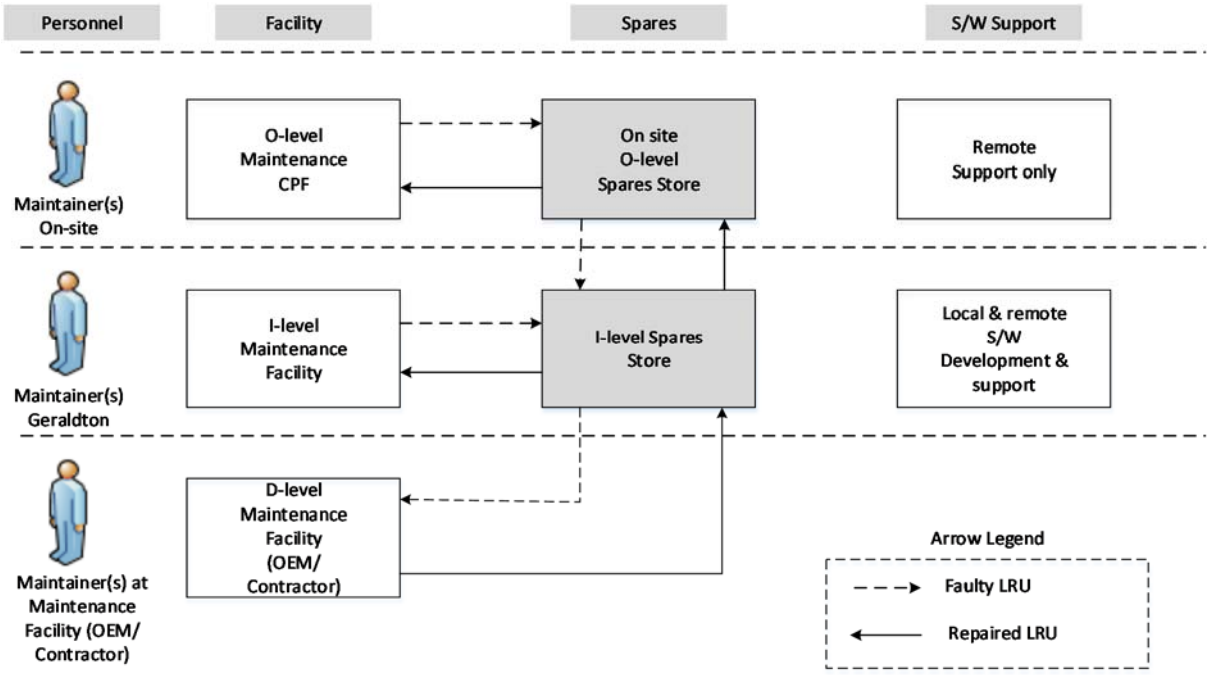


Figure 16-1 Support and Maintenance Concept

16.1.1 Support Concept

The SPS in-service support concept can be summarised as follows:

- SPS LRU spares, spare repairs, and support are provided by the construction contractor for one year after product hand-over.
- The on-site maintainer removes and replaces LRUs to restore the SPS.
- Suspect or faulty LRUs are sent to I-level for repair or replacement.
- Spare LRUs are procured and used at the I-level for simple repairs.
- Simple LRU repairs are done at the I-level, while complex or expensive repairs are fixed by contractors under warranty or maintenance contracts.
- Repaired/returned LRUs are returned via the I-level, where these are configured and tested in a realistic environment using required test equipment before being returned to the spares store.

- COTS equipment is “refreshed” at periods that are chosen to maintain support contracts for the equipment (e.g., ITE equipment typically has contracted support for only up to 5 years).

- A support contract is negotiated with the bespoke cards including the ADU and Pre-ADU signal processing boards, Cabinet and Sub-rack Management boards and Sub-rack backplane manufacturers (or another properly tooled and qualified manufacturer) to provide repair (or in the worst case, replacement) maintenance support.

16.1.1.1 *On-site Support*

On-site support includes the following:

- All maintenance actions must be done in coordination with telescope operators and operations.
- Technical personnel with the ability to remove/replace LRUs are on call to restore the SPS to full capability. Faulty equipment that operates in a redundant manner is removed and replaced at the next convenient opportunity. Faulty equipment without redundancy is replaced immediately to limit the impact on operations.
- On-site SPS consoles are used to display SPS GUIs from on-site locations to allow the maintainer, with proper authentication, to “take over” the SPS. These consoles allow maintainers to execute SPS and SPS LRU-level BIST as required. The following consoles are envisioned:
    - A CPF-based console that is permanently installed in the SPS Processing Rack (or a laptop plugged into a network port and placed on a retractable shelf) to view status and optionally control SPS and its LRUs for investigating/diagnosing and BIST execution purposes.
    - A “maintenance console” in the on-site operations room where on-site maintainers have immediate access to view status and optionally control SPS without having to enter the screened room.
    - A laptop-based console for remote maintainers to access and respond to maintenance events and queries.

16.1.1.2 *Remote and Off-site Support*

Remote off-site support personnel can use the SKAO high-speed communication network to remotely connect to the SPS. Remote users are thereby capable of performing the following operations:

- Powering down/up the entire SPS system.
- Power-cycling LRUs that are showing anomalous behaviour to correct the problem.
- Installing software and firmware upgrades.
- “Logging in” to the system via console GUIs to troubleshoot problems.
- Viewing snapshots of output data products, captured prior to output.
- Viewing other data products and statistics from monitor points.
- Additionally, off-site support personnel at the SPS I-Level support depot provide services to 1) repair LRUs that have been removed and replaced at the O-Level, 2) configure LRUs that have been replaced or sent away for repairs, and 3) verify LRUs before these are sent back to the on-site or near-to-site spares storage facility.

16.1.2 Corrective Maintenance

Corrective maintenance tasks performed on-site by the SPS maintainer include:

1. The SPS maintainer coordinates with the operations personnel to detect, isolate, and repair random unpredictable failures.
2. The SPS maintainer removes and replaces LRUs and/or performs necessary corrective actions to restore the Sub-element to operation.

16.1.3 Predictive Maintenance

Predictive maintenance tasks performed on-site include:

1. Periodically reviewing collected diagnostic information to detect equipment and components near end-of-life conditions (e.g. laser transceiver devices, disk drives, and cooling fans typically have end-of-life indicators).
2. Perform activities to restore these devices only as needed to ensure the equipment's continued operation. For example, transceivers indicating degraded performance are replaced.

16.1.4 Preventative & Scheduled Maintenance

Preventative maintenance tasks performed on-site by the SPS maintainer include:

1. Perform data backups for recovery purposes.
2. Manage storage space on data storage devices.
3. Manage operating systems' patching/updates as required.
4. Power-cycle equipment to recover from, and prevent the build-up of, conditions (e.g. operating system memory leaks) that can cause unpredicted failures.
5. On a scheduled basis, remove and replace consumables that have a limited operational lifetime (e.g., batteries, filters, and cooling fans).

The failure rate of moving parts such as bearings (contained in fans and disks) increases over time (Weibull distribution). The reliability of the Sub-element may be improved if these items are refreshed well before their predicted failure dates.

16.1.5 COTS Refresh Cycle

COTS products (hardware and software) are procured with warranty and maintenance support service agreements. Since COTS service agreements are typically up to 5 years, at least 2 COTS refresh cycles are anticipated during construction and 10 years of operations.

It is anticipated that the COTS hardware refresh activity requires some application software re-hosting, integration, and verification effort.

16.2 Spares

The SPS spare list for year 1 after acceptance is provided below. The number of spares for non-repairable items is calculated using a 95% level of confidence in reliability prediction. For repatriatable items 10% or 3 spares (whichever is lower) is assumed until a detailed simulation can be implemented to refine the numbers.

Level	Name	Product Structure	#	MTBF Specified (h)	MTTR Specified (min)	Repair-able?	Spares for 1 year
3	Cabinet Fans	Bulk	1024	80000	35	N	130
3	Cabinet Cooling	Assembly	256	500000	125	Y	3
3	Cabinet Piping and Valves	Bulk	256	500000	25	N	8

3	Cabinet PDU	Assembly	256	1000000	30	N	6
3	Cabinet Management Board	LRU	256	200000	90	Y	3
4	TPM Subrack Assembly	LRU		14900		Y	3
4	Sub-rack cooling	Bulk	2048	100000	125	Y	3
4	Sub-rack Power Supply Unit	LRU	2048	80000	30	N	249
4	Sub-rack Management Board	LRU	2048	50000	30	Y	3
4	Tile Processing Module Assembly	LRU		94716	60	Y	3
4	100 G Ethernet Data Switch (32ports_)	LRU	512	160000	55	Y	3
4	Optical Rx	N/A	131072	3054942		N	N/A
4	Pre-ADU PCA	N/A	15384	1514698		Y	N/A
4	ADU PCA	N/A	16384	1514698		Y	N/A

Table 16-1 Spares list derived from reliability prediction models.

Note that the Optical Rx, PreADU and ADU PCAs appear in the table but are not LRUs. It is assumed that the TMP module is not repairable on site.

16.2.1 COTS Equipment Repair

COTS equipment is procured with supporting maintenance contracts. Repaired or replaced LRUs are re-configured and tested under realistic conditions to confirm/prove repair.

16.2.2 Bespoke Equipment Repair

Support at the I-level includes simple LRU repairs by replacing faulty Shop Replaceable Units (SRUs) and selected plug-in-replaceable components.
An external contractor or the SKA organization provides more complex bespoke SRU (i.e. Pre ADU and Pre-ADU boards) support and repair capabilities.

16.2.3 Consumables

The UPS battery in the Control Processing Rack is a consumable item that needs to be replaced every 5 years if a UPS-unit refresh is not otherwise performed.

16.3 Support Organization

The SKA organization provides the following SPS-related support resources and services:

1. Maintains technical data under configuration control.
2. Manages the deployed configuration.
3. Provides an O-level maintainer to provide SPS on-site support.
4. Provides a spares store (and staff) close to the installed SPS.
5. Provides the I-Level depot and maintainer for SPS equipment repairs, configuration, verification, and software/firmware development/upgrade support.
6. Provides high-speed communications infrastructure for remote/off-site support.
7. Provides Failure Reporting, Analysis and Corrective Actions System (FRACAS).
8. Provides supply management support for spares/LRU repair support.

16.3.1 Technical data

Technical data age provided to develop maintenance and support manuals, operator/user's manuals, and other documents (e.g., specifications, corrective, preventive, and predictive maintenance instruction documentation, hazardous material documentation, component lists, etc.) used to support and operate SPS.

16.3.2 Obsolescence Management

SPS spares and technical support must be provided for more than 10 years after delivery. Pro-active and strategic obsolescence management of SPS equipment is performed and plans put in place to identify and mitigate the risk of parts, spares, equipment, standards, processes, skills (people), and software etc. becoming unavailable or obsolete.
The approach is in accord with the IEC/EN/BS 62402 (Obsolescence management – Application guide) or equivalent standard. Pro-active and strategic obsolescence management tasks include:

1. Performing long-term availability checks on strategic SPS equipment and components.
2. Performing analysis of the SPS BOM at defined intervals:
    a. Availability forecasts.
    b. Identification of at-risk COTS or component items.
3. Contracting COTS and critical component suppliers to provide end-of-life (EOL) notices.
4. Performing last-time and life-time buys of critical equipment and component spares.
5. Procuring support and maintenance contracts for COTS equipment and performing technology refresh activities at the end of support life.

Specifically, SPS contains complex and expensive critical components such as the FPGAs. Component vendors are requested to provide a technology roadmap to assess whether critical components will remain available for the lifetime (10 yrs.) of SPS.

16.4 Support Facilities and Equipment

SPS support requires an I-level support facility and a spares store.

16.4.1 Spares Storage

SPS requires a storage facility for SPS spares and consumables. The near-site spare storage space is specified to be a weather-protected, but not temperature-controlled storage location with no direct sunlight or water ingress into it. However, moisture or frost may condense on items contained within it.
SPS equipment requiring a special local environment and/or handling is sealed in ESD and Moisture Barrier Bags (containing a desiccant) and packaged in padded boxes for storage.
Selected spare LRUs are added to selected racks in the CPF/ RPF that have spare rack space. These LRUs are not connected to power and thus provide close-at-hand spare LRUs to reduce SPS MTTR to improve telescope operational availability.

16.4.2 Intermediate Level Support Facility

An intermediate level (I-level) support facility is used to repair, configure, test, and upgrade SPS equipment as required. The System ITF could be re-used as the SPS I-level facility.

16.4.3 Support Test equipment

The support facility at the I-level requires a test environment to check that:

1. Suspect equipment removed at the O-level indeed requires repair.
2. Repaired equipment is configured correctly.
3. Software defects have been fixed and have a low probability of introducing side effects when installed in the on-line system.

16.4.4 Computer Resources

Computer resources are required at the I-level for SPS software and firmware support tasks. The SKAO or an external contractor manages and maintains the necessary computer resources, development tools, and required licenses.

16.4.5 Accessibility and Security

The SKAO manages personnel access to the telescope's physical and electronic infrastructure. Individuals such as the SPS maintainer and remote support personnel are authorised to have physical and electronic access to specific levels required to perform their tasks.

16.4.6 Software Maintenance and Installation

Software maintenance is managed as follows:

1. After successfully completing the acceptance test phase (sell-off), SPS software is checked for conformance against the "Fundamental SKA Software and Hardware Description Language Standards" [SKA-TEL-SKO-0000661] and placed under formal Configuration Management (CM).
2. All system/software issues are raised and tracked. Subsequent software bugs, bug fixes, and OS upgrades are formally managed:
    a. Changes are approved by an SKAO Change Control Board (CCB).
    b. Software releases are checked for conformance to the "Fundamental SKA Software and Hardware Description Language Standards" [SKA-TEL-SKO-0000661].
    c. The software release is regression tested off-line as much as possible.
    d. The software release is regression tested on-line; when deployed, a key set of on-sky regression tests are run, and the results analysed – all the way through to image formation and quality analysis – before used for normal science observations.
    e. On-sky regression test failure is planned for, with previous version recovery/backup in place if needed.
3. SPS COTS equipment has both hardware and software updates during the telescope operational life. The updates are tested off-line prior to deployment and regression tested on-line after deployment (as required).
4. Bespoke LRU software should require infrequent updates. LRUs are updated to the latest software on a reboot.
5. The software development environment (e.g. design entry tool(s), libraries, compilers, debuggers, and possibly the development platform's hardware and operating system) is kept intact and maintained to the extent required to allow for maintenance in a reliable fashion.

It is not clear at this point what contractor or organization provides software maintenance.

16.4.7 Firmware Maintenance and Installation

Firmware maintenance is managed as follows:

1. After successfully completing the acceptance test phase (sell-off), firmware is checked for conformance against the "Fundamental SKA Software and Hardware Description Language Standards" [SKA-TEL-SKO-0000661] and placed under formal Configuration Management (CM).
2. Subsequent firmware bugs and bug fixes are formally managed:
    a. Changes are approved by a Change Control Board (CCB).
    b. Firmware IP blocks and, where possible, complete FPGA designs, have test benches that are PASS/FAIL self-testing. In complex I/O and processing cases the process of documenting the testing process and "golden" I/O comparisons may be used.
    c. Changes checked for conformance against the "Fundamental SKA Software and Hardware Description Language Standards" [SKA-TEL-SKO-0000661].
    d. The firmware release is regression tested off-line as much as possible.
    e. The firmware release is regression tested on-line; when deployed, a key set of on-sky regression tests are run, and the results analysed – all the way through to image formation and quality analysis – before used for normal science observations.
    f. On-sky regression test failure is planned for, with previous version recovery/backup in place if needed.
3. Bespoke LRU firmware should require infrequent updates. LRUs are updated to the latest firmware on a reboot.
4. The firmware development environment (e.g. design entry tool(s), libraries, compilers, debuggers, and quite likely the development platform's hardware and operating system) is kept intact and maintained to the extent required to allow for maintenance in a reliable fashion.

It is not clear at this point what contractor or organization provides firmware maintenance.

16.5 Manpower and Personnel

One part time O-level maintainer and 1 part time I-level maintainer are required to support SPS as outlined in previous sections.

16.5.1 Operator Role

Apart from maintenance activities, SPS is remotely monitored by a human operator although 'operated' automatically under the control of TM. The human operator(s) role is envisioned as follows:

1. The (telescope) operator has a portion of a GUI display dedicated to a rolled-up view of SPS status.
2. Faults are visually highlighted on the SPS rolled-up status display and audible alarms presented, if required.
3. The operator drills-down in successive detail to attempt to pinpoint the issue to the LRU level and may attempt to correct the fault by power-cycling/resetting one or more affected LRUs.
4. If applicable, the operator can bring on-line the standby FSP-UNIT thereby bypassing an FSP fault.

5. The operator has a 24/7 hot-line to maintenance personnel to report issues that cannot be corrected in such a manner.
6. On-call maintenance personnel with equipment, spares, and authorization assess the fault and do repairs as needed.

16.5.2 On-site Maintenance Support Role

The on-site maintainer performs preventative, predictive, and corrective maintenance tasks such as removing and replacing faulty LRU equipment to restore SPS to keep it operational.
Educational and training requirements for on-site or O-level maintenance support personnel are:

1. Must have a qualified electronic technician education level.
2. Must have sufficient experience in computer system maintenance and repairs.
3. Must complete a training course to operate, support, and maintain SPS.

This maintainer's primary objective is to detect and isolate faulty LRUs (corrective maintenance) and to remove and replace these to restore SPS to full functionality. The maintainer's secondary objective is to determine what maintenance needs to be scheduled (predicted and preventative maintenance) and to coordinate and perform required tasks when scheduled.

16.5.3 Off-site Maintenance Support Role

The off-site maintainer performs second line equipment maintenance (I-level) functions, including LRU repair via SRU swapping and associated testing. Educational and training requirements for the SPS I-level maintainer are:

1. Must have a qualified electronic technician education level with software specialization.
2. Must have sufficient experience in computer system maintenance, software updates, and repairs.
3. Must complete a training course to support and maintain SPS equipment, including SRU swapping.

The off-site maintainer performs relatively simple diagnostics to pinpoint the failure items in LRUs. The maintainer configures, and tests all repaired or upgraded equipment in a representative environment to verify that it is correctly configured and fully operational before being returned to the spares store.

16.5.4 Maintainer Training and Training Support

The SPS contractor provides manuals, training materials, and training courses to the O-level and I-level maintenance and support staff to support SPS operations.
SPS operation training is also provided to the telescope operator, but at the level of understanding what GUI-display indicators mean and how to interpret them, as well as what actions to take to attempt clear faults in the operational system.
Annual refresher training sessions are provided to the operators/maintainers as required.

16.6 Packaging, Handling, Storage and Transportation

A Packaging, Handling, Storage, and Transportation report is provided during construction to describe formats, procedures and methods to ensure that:

1. Packaging provides adequate protection against corrosion, deterioration, and physical damage during shipment and handling from source to destination.

2. Equipment is marked correctly (e.g., Serial Number, Part Number).
3. Adequate shipment and storage instructions are provided to prevent shipment delays.

16.6.1 Equipment Labelling and Configuration Management

SPS equipment is marked/labelled with electronically readable identification information as follows:

1. Equipment, bespoke and COTS, is labelled with name, part number, and serial number.
2. Interfaces, on bespoke and COTS items, are labelled at the generic/general LRU-use level (i.e. labelled according to function rather than placement/use in the system).
3. Cables are labelled according to their specific use in the SPS system. Cable labels are placed within 10 cm of the cable end and indicate the destination Rack/LRU/Interface number, as well as the source Rack/LRU/Interface number.

SPS equipment labelling is in a conspicuous location, viewable when items are removed or when they are installed in their intended operating environment. Labels are affixed so that they are unlikely to come off during storage, maintenance, or normal operation for a period of at least 10 years after manufacture. Disposable LRUs, if any, are labelled as such.

A report is provided that details the equipment naming and labelling strategy. The report also details labelling items that are packaged for transportation and storage (e.g. packages are labelled with their part and serial numbers).

As appropriate, labels are affixed to rack front and/or rear inside panels or doors to show the layout of rack components, connections, etc. This allows maintenance personnel to have immediate access to information needed for maintenance without having to track down manuals etc.

17 Appendix A Requirements and Design Traceability Matrix

Table 17-1 lists all the SKA1-LFAA_SPS_REQ-<id_num> (shortened to "L3-<id_num>") requirements, indicates if the design described in this DDD is believed to be Compliant, Non-compliant, or Partial, and provides compliance rationale as a trace to one or more sections in this document where compliance is explained.

L3-184	**SPS number of SKA1_Low stations** When commanded, SPS shall accept and process inputs for both polarisations from all 256 antenna within up to 512 Field Nodes in the SKA1_Low array, each with an identical interface defined in the SPS to Field Node ICD
Compliant	Compliant
Compliance Rationale	DDD Section 5.2
L3-185	**SPS maximum array extent** SPS shall process data from Field Nodes with separations as large as 65 km.
Compliant	Compliant
Compliance Rationale	DDD Section 5.1.1
L3-174	**Digitisation** Digitisation of LFAA antenna signals shall be to at least 7.8 ENOB (equivalent number of bits).
Compliant	Compliant
Compliance Rationale	DDD Section 5.2, 5.4.1.2
L3-175	**SPS dynamic range** The amplitude dynamic range of the SPS signal chain shall be such that for the SKAO supplied RFI uses Cases the signal level is within the linear region as per linearity requirements 95% of the time.
Compliant	Non-compliant
Compliance Rationale	Compliance cannot be identified until the SKAO supplied RFI Use cases are made available. However, the design has taken all reasonable measures to minimise the occurrence of clipping
L3-227	**SPS coherence loss** The SPS signal and clock distribution chain shall cause a maximum differential variation of no more than 0.2 deg phase or 1.4 ps time in the signal and clock distribution chains for periods of 1 second to 1 minute
Compliant	Compliant
Compliance Rationale	DDD Section 5.2.2.3
L3-203	**Linearity** The level of spurious products generated by SPS, in the presence of signals representative of the expected RFI [AD37] environment shall maintain the degradation of expected thermal noise floor within 10% over an integration period of 1000 hours.
Compliant	Non-compliant
Compliance Rationale	The requirement is identified as being non-compliant until the definition of the parent requirement has been resolved.
L3-207	**SPS signal processing signal to noise**

	LFAA.SPS shall keep the degradation of its Signal to Noise ratio to less than 2 % compared to ideal processing for the same inputs.
Compliant	Compliant
Compliance Rationale	DDD Section 6.2.2 & 6.5
L3-173	**SPS Instantaneous bandwidth** LFAA.SPS when commanded by the MCCS, shall process up to and including 300 MHz of aggregate bandwidth per polarisation, as discrete coarse channels individually assigned to sub-stations and/or beams, for a given observation period or until commanded to stop.
Compliant	Compliant
Compliance Rationale	DDD Section 5.1.1, 5.2.1, 6.2, 6.4.1
L3-198	**SPS RFI detection and flagging** When commanded, SPS shall automatically detect RFI in the processed bandwidth and, when detected, flag data to prevent corruption of any downstream data products. Conformance to this requirement is determined by testing of all SKAO-mandated RFI use cases such that, in each case, prescribed acceptable performance is obtained.
Compliant	Non-compliant
Compliance Rationale	Compliance cannot be stated until the SKAO provided RFI Use Cases are made available. However, the flexibility of the design with respect to configurable threshold and integration period should give reasonable confidence that the requirement can be met. DDD Section 3.1, 5.1.1, 5.1.2, 5.2, 5.5.2, 6.3.4, 6.5, 6.8, 7.2.4, 9.1.3
L3-199	**SPS RFI masking** LFAA.SPS shall flag beamformed data corrupted by RFI using a mask provided by TM via MCCS, with a time resolution of the integration unit and a frequency resolution of one coarse channel.
Compliant	Compliant
Compliance Rationale	DDD Section 3.1, 5.1.1, 5.1.2, 5.2, 5.5.2, 6.3.4, 6.5, 6.8, 7.2.4, 9.1.3
L3-200	**Saturated Data Flagging** LFAA.SPS shall flag individual pre-channelised samples within the data stream exceeding a MCCS supplied value representing the boundary of acceptable saturation.
Compliant	Compliant
Compliance Rationale	DDD Section 5.1.1
L3-221	**SPS spectral channels** For each polarisation of each antenna, SPS shall form a fixed number of least 350 and no more than 512, dependent on implementation, linearly spaced frequency channels across the frequency band
Compliant	Compliant
Compliance Rationale	DDD Section 6.3, 6.3.2 Compliant through design.
L3-208	**Oversampling**

	SPS frequency channels shall have a sampling frequency equal to the channel separation (nominal channel bandwidth) multiplied by an oversampling factor not larger than 1.20.
Compliant	Compliant
Compliance Rationale	DDD Section 6.3.2
L3-181	**SPS channelisation transition band for adjacent frequency channels** The transition band between the SPS coarse frequency channels shall be monotonically decreasing starting from the coarse channel edge plus 1/128 of its bandwidth, to -60 dB or better at the nominal coarse channel edge as aliased in the oversampled channeliser.
Compliant	Compliant
Compliance Rationale	DDD Section 6.3.4
L3-182	**SPS channelisation maximum leakage for non-adjacent frequency channels** The upper envelope of the power of noise leaking for non-adjacent visibility spectra coarse frequency channels shall fall off as 1/f or better as a function of frequency offset from the centre of a given frequency channel, for frequency offsets up to half the input bandwidth.
Compliant	Compliant
Compliance Rationale	DDD Section 6.3, 6.3.2
L3-183	**SPS channelisation frequency channel amplitude response** The amplitude response of the LFAA SPS channeliser shall have a spectral slope of less than 0.003 dB per imaging zoom frequency channel across each LFAA channel passband. If the response covers more than one imaging zoom channel (overlapping region) the requirement applies to the sum of the power responses of the overlapping channels..
Compliant	Compliant
Compliance Rationale	DDD Section 6.3.3
L3-202	**Total noise leakage power** The maximum total noise leaked from all channels into each LFAA channel, excluding the two adjacent channels on each side, shall be less than 60 dB.
Compliant	Compliant
Compliance Rationale	DDD Section 6.3.4
L3-209	**SPS Spectral Purity** The spectral distortion of SPS beams compared to an ideal beamformer provided with the same inputs, shall be less than -60 dB in amplitude and 0.001 radians in phase.
Compliant	Compliant
Compliance Rationale	DDD Section 6.4.2 & 6.5
L3-180	**SPS Autocorrelation spectra** LFAA.SPS shall compute autocorrelation spectra for individual antennas over the whole observing band (one antenna at each time), or for station beams over the beamformed spectral regions, with resolution of one coarse channel and time resolution of better than a LFAA calibration cycle.
Compliant	Compliant

Compliance Rationale	DDD Section 5.5.1 & 5.5.4
L3-178	**Beam steering** SPS shall, when commanded, track delays on individual antennas with an accuracy of better than 1.70 ps given delay and delay rate values from MCCS.
Compliant	Compliant
Compliance Rationale	DDD Section 6.4.2
L3-177	**SPS Multi-beam capability** LFAA.SPS shall, when commanded, generate up to eight beams per station or substation with independent pointings such that the sum of bandwidths over these beams is less than or equal to the available bandwidth. For Stations the available bandwidth is 300MHz, for 1024 substations across the telescope 150 MHz and 2048 substations across the telescope 75MHz.
Compliant	Compliant
Compliance Rationale	DDD Section 6.4.1, 6.4.2 & 6.4.3
L3-201	**Multiple beam widths** LFAA.SPS shall, when commanded, form multiple station beams. Each beam will have divergent pointing and is formed by an independent channel selection (where independence allows identical, overlapping or non-overlapping). Each selection is composed of a multiple of 8 channels, starting at an even channel number.
Compliant	Compliant
Compliance Rationale	DDD Section 6.4, 6.4.1 & 6.4.2
L3-225	**Support for sub-stations** The SPS shall be configurable for the control and monitoring of up to 2048 sub-stations, configured within the limits set out in section 5.7.1 of [AD38]. Representative cases include but are not limited to the following (see document for further explanation): a. 1024 sub-stations randomly distributed within field nodes. i. Stations are populated with 4 randomly-located sub-stations in the core and 4 randomly-located sub-stations in one of the 6 field nodes at each cluster location. ii. 75 MHz of bandwidth is available. b. 1024 sub-stations regularly distributed within field nodes. i. Stations are populated with 6 sub-stations in the core and 4 sub-stations in one of the 6 field nodes at each cluster location. ii. 75 MHz of bandwidth is available c. 2048 sub-stations randomly distributed within field nodes i. Stations are populated with 4 randomly located sub-stations in all of the 512 field nodes. ii. 19 MHz of bandwidth is available. d. 2048 sub-stations regularly distributed within field nodes. i. Stations are populated with 6 sub-stations in the core and 6 sub-stations in 3 of the 6 field nodes at each cluster location ii. 19 MHz of bandwidth is available.
Compliant	Partial

Compliance Rationale	75MHz for 6 substations exceeds 300 MHz bandwidth. Others are compliant DDD Section 6.4.1
L3-226	**SPS processing latency** The SPS shall have latency of at most 10 ms from the time that a signal arrives from the Field Node to the time when the beamformed signal is forwarded to CSP.
Compliant	Compliant
Compliance Rationale	DDD Section 9.2.3
L3-228	**SPS polarisation isolation** The SPS shall have an isolation between any individual polarisation pairs for individual antennas of greater than 30dB in total across the processing chain
Compliant	Compliant
Compliance Rationale	The requirement is expected to be compliant through design
L3-229	**SPS relative gain tolerance** The station beam accuracy for the SPS, over a 10-minute interval shall have a relative gain tolerance of better than 0.2%, across the LFAA frequency range.
Compliant	Compliant
Compliance Rationale	DDD Section 9.4.4
L3-213	**Data forwarding for transient capture** The SPS, when commanded, shall forward streamed station beam data at its native time and frequency resolution to MCCS for fast transient capture configured by MCCS for: 1. channel selection of up to a total of 150 MHz which may differ between beams 2. a selected station beam set. **3.** a data width of 2, 4 8 bits
Compliant	Compliant
Compliance Rationale	DD Section 6.5, 6.7, 6.7.1
L3-179	**Synchronous Time Stamping** Each station beam shall provide to the correlator-beamformer data block time stamps, synchronous with and locked to the sample clock and deterministically related to 1PPS, within an accuracy of 1.5ns (1σ) of the 1PPS distribution.
Compliant	Compliant
Compliance Rationale	DDD Section 5.2.2
L3-222	**Network Time Protocol** All SPS client devices and applications that require synchronised telescope network time shall comply with the Network Time Protocol version 4 standard, RFC 5905
Compliant	Compliant
Compliance Rationale	DDD Section 5.2.2.1 & 5.2.2

L3-186	**SPS status** When commanded, SPS shall provide the following status information to MCCS: (a) internal temperature; (b) voltage; (c) power; (d) cooling mechanism status; (e) communication path status; (f) device configuration status;
Compliant	Compliant
Compliance Rationale	DDD Section 3.2.3, 3.3 5.1.1, 5.2.1, 5.4.2, 5.4.3, 5.4.4, 6.9
L3-187	**SPS alarm latency** SPS shall indicate an alarm within 0.6 seconds from the time a measurement crosses an alarm set-point.
Compliant	Compliant
Compliance Rationale	DDD Section 9.2, 9.2.2
L3-188	**SPS processing resource configuration or reconfiguration time** When commanded, unless otherwise required, SPS shall complete any signal processing configuration or reconfiguration, within 24 seconds TBC from the specified configuration or re-configuration start time.
Compliant	Compliant
Compliance Rationale	DDD Section 9.2.1
L3-189	**SPS station beam weighting** When commanded, SPS shall apply independent dynamic weights to each antenna contributing to each station beam, including the ability to exclude individual antennas. Note: weights will come from MCCS.
Compliant	Compliant
Compliance Rationale	DDD Section 5.5.4, 6.6.1.3, 6.4 6.4.1, 6.4.2 & 6.5
L3-190	**SPS processing status reporting** When commanded, SPS shall report at least the following processing status: 1. Configuration for any antenna's processing path, 2. Function Mode for any TPM, 3. Antenna inclusion in any processing operation and output data production and **4.** any accumulated/stored exception or inconsistency-detection conditions.
Compliant	Compliant
Compliance Rationale	DDD Section 5.1.1, 5.2.1, 5.4.2, 5.4.3, 5.4.4
L3-191	**SPS to Field Node General**

	The interface between SPS and Field Node shall be compliant with the SKA1 SPS to Field Node Sub-elements Interface Control Document [SKA-TEL-LFAA-0200030].
Compliant	Compliant
Compliance Rationale	DDD Section 6.1, 5.3.4, 5.3.5
L3-192	**MCCS to SPS General** The interface between SPS and MCCS shall be compliant with the SKA1 MCCS to SPS Sub-elements Interface Control Document [SKA-TEL-LFAA-0200030].
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4, 5.3.5, 5.4.3, 6.1
L3-214	**MCCS to Field Node M&C message forwarding** The SPS shall forward all monitoring and control messages between the MCCS and Field Node in accordance with the MCCS to SPS and SPS to Field Node ICDs
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4
L3-145	**LFAA to CSP: General** The interface between LFAA and CSP shall be compliant with the SKA1 LFAA to CSP Interface Control Document [100-000000-004].
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4
L3-223	**Beam Identification** THE SPS shall uniquely identify beam data products with the beam and the station they are associated with in accordance with the LFAA to CSP ICD.
Compliant	Compliant
Compliance Rationale	Compliant by design
L3-146	**SADT to LFAA: General** The interface between SADT and LFAA shall be compliant with the Low SADT to LFAA Interface Control Document [100-000000-026]
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4
L3-147	**LFAA to Infra Interface** The interface between SPS and Infra AUS shall be in compliance with the latest approved version of the SKA1 LFAA to INFRA Interface Control Document [100-000000-003]
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4
L3-148	**SPS deployment location** SPS shall be located in the Central Processing Facility and Remote Processing Facilities in accordance with the latest approved version of the LFAA to INFRA ICD [100-000000-003]
Compliant	Compliant

Compliance Rationale	DDD Section 5.3.4
L3-168	**SPS safety legislation and regulations** SPS equipment and operations shall comply with all applicable Australian Occupational Health and Safety legislation and regulations in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-169	**SPS safety certification** SPS rack and LRU equipment shall be safety certified to AS/NZS 60950.11:2015 or equivalent in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 11.6
L3-210	**[Useful] LFAA.SPS environmental certification** LFAA.SPS rack and LRU equipment shall be RoHS 2 (2011/65/EU) certified in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-170	**SPS rack side-to-side stability** SPS racks shall be attached to adjacent racks in the same row to provide lateral stability in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 5.4.5, 11.7
L3-171	**SPS rack forward-backward stability** SPS racks shall have a Centre of Gravity (CofG) that is less than 50% of the rack height in the upward direction in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-211	**[Useful] LFAA.SPS acoustic noise emission** [Useful] LFAA.SPS acoustic noise emission sound pressure level shall be in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 11.2.7, 11.7 If the SPL is exceeded, warning labels and ear defenders can be utilised.
L3-172	**SPS equipment shutdown on failure** SPS shall autonomously detect and shut-down affected equipment in accordance with the latest approved version of the LFAA to INFRA ICD, when any of the following conditions occur: 1. an over-current condition occurs in a rack; **2.** an over-temperature condition occurs in an LRU.

Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-193	**SPS rack size** SPS shall use racks with dimensions of less than or equal to 800mm wide x 1200mm deep x < 2000mm floor to top of cabinet in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4
L3-194	**SPS rack weight** The mass of fully populated SPS racks shall not exceed 620 kg in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4
L3-195	**SPS rack count** The SPS rack count shall not exceed 148 in the CPF and 3 in each of the 36 RPFs in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 5.3.4
L3-149	**SPS power quality** SPS shall operate in compliance with the SKA1 Power Quality Standard Specification [SKA-TEL-SKO-00000293] in accordance with the latest approved version of the LFAA to INFRA Interface Control Document [100-000000-003].
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-151	**SPS power factor** For 20% to 100% loading SPS rack equipment shall have a power factor between 0.9 lagging to 0.95 leading in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-150	**SPS phase current balancing** The SPS electrical load shall be balanced such that the difference in currents between any two of the three phases will nominally be less than 5% and not exceed 10% for periods greater than 2 minutes when the sub-element is fully powered in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 9.5.1
L3-152	**SPS average power consumption** SPS average power consumption shall not exceed 1226 kW in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Non-compliant

Compliance Rationale	DDD Section 9.3. The SPS sub-element forms the largest power consumer in the LFAA. The allocated power budget for AA4 is 1636 kW. The station will be nominally 350kW and the MCCS ~ 60kW, this suggests an allocation of ~ 1226 kW for SPS. The calculated power consumption is 1360kW. Consequently, the SPS is ~ 8% over budget and consequently non-compliant
L3-153	**SPS power draw rate of change** SPS power draw rate of change shall be less than 20% of the maximum power draw averaged over a one second interval (TBC) during start up and mode transitions in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 9.5.2 9.5.3 Power rate of change is controlled through sequenced power up and power down
L3-220	**SPS harmonic current limits** SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEEE 519-1992 part 11.5standard or equivalent for Harmonic Current Limits under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4 SPS is expected to be compliant to this specification. COTS to be procured to meet this spec and develop products that connect to facility power will be certified by an internationally recognised EMC compliance testing contractor. The PQ document is more constraining on the SPS design.
L3-154	**SPS rack power interface** Each LFAA.SPS rack shall connect to two INFRA Element CPF electrical power outlets via two 3 phase power cables (length >=2 meters) that have IEC 60309 (6H) 3P+N+PE 32A RED Cable Mount Plugs (Part Number: 888-231-NS).
Compliant	Compliant
Compliance Rationale	DDD Section 9.6
L3-155	**SPS rack peak power draw** SPS racks shall have a peak power draw of less than 1226 kW in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Non-compliant
Compliance Rationale	DDD Section 9.3. The peak power is limited to the average power. The power up sequence ensures this is the case. As with the average power it is ~ 8% over budget
L3-156	**SPS rack short circuit current survivability** SPS rack electrical protection circuitry shall have an Interrupt Rating (IR) and Short-Circuit Current Rating of not less than 25 kA TBC in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 5.4.4
L3-157	**SPS rack safety earth connection** SPS racks shall have a safety earth connection point with a connection resistance of less than 0.1 Ohm as per the latest approved version of the LFAA to INFRA ICD
Compliant	Compliant

Compliance Rationale	DDD Section 5.4.5
L3-215	**SPS inrush current** The LFAA.SPS shall have an inrush current of less than three times the average current draw at the point of connection at any point of time and should reach the steady state current value within one second after switching on.
Compliant	Compliant
Compliance Rationale	Power sequence manages the larger aspects of the situation and the power units will be procured for compliance. Each TPM has an individual controller for fine granularity of power control including hot swap. DDD Section 9.5.2 9.5.3
L3-216	**LFAA.SPS phase operability (voltage)** The LFAA.SPS shall be operable with supplied voltage phase with a variation of up to 2% of the nominal voltage and 3% during unusual network and load configurations.
Compliant	Compliant
Compliance Rationale	DDD Section 9.5.1
L3-217	**SPS operable frequency** The LFAA.SPS shall be operable inside the following frequency deviation: 1. From Grid supply ± 2% (49Hz to 51Hz) **2.** From Generating plant supply ± 5% (47.5 to 52.5 Hz)
Compliant	Compliant
Compliance Rationale	The design is expected to be compliant, but this has not been checked yet and isn't documented in the DDD yet. However, the requirement is fairly standard for COTs equipment. For example, the selected power supply for the aux power in the cabinet (Meanwell DRP-240) accepts 47-63 Hz, i.e. 50-60 Hz +/- 5%.
L3-218	**Magnitude of supply voltage (steady state)** The LFAA.SPS shall operate with supply voltage within ± 10% (360V - 440V)
Compliant	Compliant
Compliance Rationale	Procure power equipment to meet this specification
L3-219	**Supply voltage transients** The LFAA.SPS shall be withstand the transient limits defined in IEC 62040-3 dynamic output performance classification 3
Compliant	Compliant
Compliance Rationale	Procure supplies to be compliant with standard.
L3-158	**SPS harmonic current emissions** SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-3-2 standard or equivalent for Harmonic Current Emissions under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4 SPS is expected to be compliant to this specification. COTS to be procured to meet this spec and develop products that connect to facility power will be

	certified by an internationally recognised EMC compliance testing contractor. The PQ document is more constraining on the SPS design.
L3-159	**SPS voltage fluctuations and flicker emissions** SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-3-3 standard or equivalent for Voltage Fluctuations and Flicker Emissions under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-160	**SPS number of electromagnetic radiators** SPS shall contain at most 4500 LRUs in the CPF and 50 in the RPF that radiate EMI at levels up to CISPR 22/32 or equivalent standard in the SKA Low telescope frequency range. Note: Rack level LRUs must be configured as per the LFAA design during radiated emissions certification. In other words, rack level LRUs must be populated with all components that contribute radiated emissions. If some components aren't present during certification, these components must be separately certified and be accounted for in the emitter count as specified above.
Compliant	Compliant
Compliance Rationale	DDD Section 12.3.5.1
L3-161	**SPS ESD immunity** SPS equipment susceptible to ESD shall be compliant with the IEC 61000-4-2 standard or equivalent standard for ESD immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-162	**SPS radiated, radio-frequency, electromagnetic field immunity** SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-3 standard or equivalent for radiated, radio-frequency, electromagnetic field immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-163	**SPS electrical fast transient/burst immunity** SPS equipment connected to the CPF electrical network shall be compliant with the IEC 61000-4-4 standard or equivalent for electrical fast transient/burst immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-164	**SPS surge immunity**

	SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-5 standard or equivalent for Surge immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4 SPS is expected to be compliant. COTS to be procured to meet this spec and develop products that connect to facility power will be certified by an internationally recognised EMC (to CISPR 22 or equivalent) compliance testing contractor. The PQ document states that INFRA AU may only provide protection from surges larger than 2.5kV, CISPR will only check protection to class 3 or to 2kV
L3-165	**SPS immunity to conducted disturbances induced by radio-frequency fields** SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-6 standard or equivalent for immunity to conducted disturbances, induced by radio-frequency fields under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-166	**SPS power frequency magnetic field immunity** SPS equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-8 standard or equivalent for power frequency magnetic field immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-167	**SPS voltage dips, short interruptions and voltage variations immunity** SPS LRU equipment connected to the CPF and RPF electrical network shall be compliant with the IEC 61000-4-11 standard or equivalent for voltage dips, short interruptions and voltage variations immunity under standard test conditions and setups in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-196	**SPS sub-element thermal load** The SPS total thermal load shall not exceed 1636 kW in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Compliant
Compliance Rationale	DDD Section 9.3, 9.4.2
L3-197	**SPS rack thermal load** The thermal load of SPS racks shall be less than 5 kW in accordance with the latest approved version of the LFAA to INFRA ICD.
Compliant	Non-compliant
Compliance Rationale	DDD Section 9.3, 9.4.2

L3-61	**SPS software and quality** SPS software and hardware description language related deliverables shall comply with the "Fundamental SKA Software and Hardware Description Language Standards" [RD2]
Compliant	Partial
Compliance Rationale	Partial compliance for the delivered SW/FW. Software/firmware has been written using good software practice rules, some of the modules have associated regression tests, but some work is needed to have everything aligned to RD1. Current code is however to be considered demonstration code, not the final delivered product. Statements regarding current SW/FW state have been added to DDD sections 5.5. and 5.6. The Plan to comply is included in DDD sections 16.4.6 (software) and 16.4.7 (firmware). Regression tests are described in 13.3
L3-31	**SPS Low power state** SPS shall have a low power mode that reduces the power consumption to less than 5% of the nominal power requirement.
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.5
L3-32	**Low power mode on power application** SPS shall enter the "low power" mode on start-up and remain in Low Power mode until commanded otherwise
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.1
L3-88	**SPS Low Power Mode capabilities** SPS shall continue to communicate with MCCS, monitor, report status and execute received commands while in the Low Power Mode
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.1
L3-73	**SPS occupational health and safety** SPS shall comply with all local occupational health and safety regulations applicable to the Australian observatory and its operations.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-65	**SPS hazard elimination** SPS shall be safe to the operators, maintainers and own equipment with categorization exceeding the acceptable levels defined in the SKA Project Safety Management Plan [AD12].
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-68	**SPS fail-safe operation** SPS equipment shall operate in a locally fail-safe manner and not rely on external safety devices or measures to operate safely.
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.6.2, 11.5, 11.7

L3-69	**SPS non-propagation of failures** SPS equipment hardware failures and software errors shall be safe from creating hazardous conditions in interfacing elements and sub-elements.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-48	**SPS fail safe state** SPS equipment that would otherwise present a safety hazard when subjected to an unplanned loss of main electrical power or main control function, shall enter a designated fail-safe state.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-49	**SPS fail safe warnings** Where transitioning to a designated fail-safe state represents a hazard, components of the SPS shall issue continued warnings for the duration of the transition.
Compliant	Compliant
Compliance Rationale	DDD Section 11.5
L3-50	**SPS fail safe recovery** Once a transition to a designated fail-safe state is triggered, the SPS shall complete the transition and remain in the designated fail-safe state until commanded otherwise.
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.6.2, 11.5
L3-89	**SPS protruding obstacles** SPS equipment LRUs and racks shall eliminate or suitably protect obstacles that protrude and that may cause a safety hazard to personnel or equipment.
Compliant	Compliant
Compliance Rationale	DDD Section 5.4
L3-90	**SPS sharp edges and corners** Exposed SPS shall have: • corners rounded to a radius not less than 13 millimetres or suitably protected with covers or coatings; • sharp edges rounded to a radius not less than 0.75 millimetres.
Compliant	Compliant
Compliance Rationale	DDD Section 5.4
L3-91	**SPS heavy equipment handholds** SPS equipment weighing more than 23 kg shall have lifting provisions to allow team lifting and/or the use of moving equipment.
Compliant	Compliant
Compliance Rationale	DDD Section 5.4
L3-92	**SPS heavy equipment lifting arrangement**

	SPS equipment with a weight of more than 40 kg shall have an integral lifting arrangement to allow mechanical assisted lifting.
Compliant	Compliant
Compliance Rationale	DDD Section 5.4
L3-93	**SPS electrical installation** The electrical wiring of all SPS hardware shall comply with low voltage installation Standards (wiring of premises) AS/NZS 3000:2007.
Compliant	Compliant
Compliance Rationale	Safety - see Section 11.3.2 - Power supply and wiring demonstrate SPS hardware wiring complies to relevant Australian electrical standards.
L3-94	**SPS electrical circuit interlock** The SPS shall provide electrical circuit inter-locks to prevent personnel coming into contact with hazards that cannot otherwise be eliminated from design.
Compliant	Compliant
Compliance Rationale	Safety - see Section 11.3.1 - SPS expect only trained personnel to access to racks for installation and maintenance. Electrical and optical hazards are enclosed (although not locked). For in internal optical connections there are automatic shutters (mechanical interlock). For electrical there are no interlocks present but all connection to INAU are via 3-phase 400V plugs. These plugs can be disconnected to render the hardware safe.
L3-95	**SPS Thermal Overload Protection** All LRUs within SPS shall be equipped with thermal overload protection functionality to automatically power down the LRU when the SPS operating temperature exceeds the LRU's safe operating temperature.
Compliant	Compliant
Compliance Rationale	Scenarios - Section 7.3 - SPS LRU's contain an automatic thermal overload protection to autonomously power down (when exceeding a programmable pre-set temperature).
L3-96	**SPS safety of equipment** SPS racks and equipment shall comply with IEC 60950-1 Information Technology Equipment - Safety Part 1 General Requirements or equivalent standard.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-97	**SPS power interruption survivability** SPS racks shall survive a main power interruption at any time, without requiring a repair activity to restore it once power is restored.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-98	**SPS LRU electrostatic warning marking** SPS LRU equipment with electrostatic sensitive components shall be fitted with ESD warning labels.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-99	**SPS equipment identification and safety markings**

	SPS equipment shall in accordance with ISO 61310_2 or equivalent bear all markings necessary: • for its unambiguous identification; • for its safe use; and supplementary information given, as appropriate: 1. permanently on the machinery; 2. in accompanying documents such as instruction handbooks; **3.** on the packaging.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-100	**SPS heavy equipment weight warning** SPS LRUs weighing more than 23 kg shall have a Weight Warning label.
Compliant	Compliant
Compliance Rationale	DDD Section 11.4.3
L3-101	**SPS hazard warning marking** SPS equipment that presents a potential hazard shall display a label in accordance with ISO 7010 or equivalent.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-102	**SPS label robustness** SPS labels shall be affixed for at least 50 years or the lifetime of the equipment, whichever is the smaller, and unlikely to come off during maintenance or as a result of the environment.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-63	**SPS environmental protection regulations** SPS shall be compliant with all local, State and national environmental protection legislation and regulations.
Compliant	Compliant
Compliance Rationale	Safety - see Section 11.7 - SPS design is maximizing the usage of environmentally friendly materials in the design in order to be compliant with Australian environmental protection legislation.
L3-103	**SPS recycling and decomposition.** SPS equipment shall be compliant with environmental, ecological, safety, political and social legislation with regard to recycling and decomposition.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-104	**SPS disposable equipment labelling** SPS disposable equipment should be labelled as such.
Compliant	Compliant

Compliance Rationale	DDD Section 11.7
L3-105	**SPS restriction of hazardous substances** SPS shall be compliant with the RoHS Directive 2011/65/EU (RoHS 2) or equivalent.
Compliant	Compliant
Compliance Rationale	DDD Section 11.7
L3-106	**SPS EMI and EMC** SPS equipment shall be compliant with the emission and immunity standards in the SKA EMI/EMC Standards and Procedures [SKA-TEL-SKO-0000202] document.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-107	**SPS essential conducted and radiated electromagnetic emissions** SPS LRU equipment that radiate electromagnetic emissions in the SKA1 frequency range and that aren't within a shielded enclosure of a higher level LRU, shall at a minimum be compliant with the IEC 61000-6-4 standard or equivalent for conducted and radiated emissions under standard test conditions and setups in the SKA Low telescope frequency range as specified in the SKA EMI/EMC Standards and Procedures [AD41].
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-108	**SPS electromagnetic susceptibility** SPS equipment shall be compliant with the IEC 61000-6-2 standard or equivalent for susceptibility to conducted and radiated emissions under standard test conditions and setups. Note: Only LRUs with electrical or electronic components that are susceptible to EMI and that aren't within a shielded enclosure of a higher level LRU need to be checked for compliance.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-109	**SPS essential off-the-shelf equipment EMC marking** SPS "off-the-shelf" LRU equipment shall as a minimum be CISPR 22 and 24 Class A or equivalent compliant over the SKA telescope frequency range.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-110	**SPS electricity network electromagnetic compatibility** SPS equipment shall follow the code of practice for the application of Electromagnetic Compatibility (EMC) standards and guidelines in electricity utility networks.
Compliant	Compliant
Compliance Rationale	DDD Section 12.4
L3-111	**SPS Inherent Availability**

	SPS shall have an Inherent Availability (Ai) of at least 99.99% while operationally capable.
Compliant	Compliant
Compliance Rationale	DDD Section 10.2.2, 10.3
L3-112	**SPS Operationally Capable** SPS shall remain Operationally Capable when any one processing LRU fails.
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.6.3
L3-113	**SPS maintenance hours** SPS shall require less than 150 Direct Maintenance Hours (DMH) per month at the Organizational Level (O-Level). Note: DMH/month = MTTR x number of equipment repair actions per month at the O-Level.
Compliant	Compliant
Compliance Rationale	DDD Section 10.3
L3-114	**SPS mean time to repair** SPS shall have a Mean Time to Repair (MTTR) of less than 1 hour at the organizational level (O-Level).
Compliant	Compliant
Compliance Rationale	DDD Section 10.3
L3-115	**SPS software maintenance down time** SPS shall have a Maintenance Down Time (MDT) of less than 1 hour per year for software repairs (during steady state operation). Note: Software MDT is defined as the time per year that SPS is unavailable as result of SPS software defect repairs and software maintenance activities during the telescope operational phase. SPS software defect repairs and maintenance that don't require SPS down-time are excluded from MDT.
Compliant	Compliant
Compliance Rationale	DDD Section 10.3All reasonable efforts are being made in the SPS design to allow software maintenance without downtime, however, more information is required on how software maintenance will be performed during operations.
L3-116	**SPS off-line built-in self-test capability** When commanded and with the SPS Administrative Mode set to OFFLINE, SPS shall perform diagnostic tests to detect and isolate LRU and sub-element level faults.
Compliant	Compliant
Compliance Rationale	DDD Section 6.9
L3-117	**SPS off-line fault detection performance** When commanded and the SPS Administrative Mode set to OFFLINE, SPSF built-in diagnostic self-test capability shall detect and report 99% of all critical sub-element failures. Note: A Critical Failure is a failure that would prevent SPS being "Operationally Capable".

Compliant	Compliant
Compliance Rationale	DDD Section 10.3 All SPS faults identified in the FMECA can be detected. There is no further analytical proof of compliance at this time.
L3-118	**SPS off-line fault isolation performance** When commanded and with the SPS Administrative Mode set to OFFLINE, SPS shall isolate 95% of all failures down to an LRU level. Note: The SPS maintainer functions as part of the fault isolation mechanism by removing and replacing suspect LRUs.
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.6 All SPS faults identified in the FMECA can be isolated to one LRU with assistance from the maintainer. No further analytical proof of compliance at this time.
L3-119	**SPS off-line communications fault detection** When commanded and with the SPS Administrative Mode set to OFFLINE, SPS shall detect and report 99% of sub-element LRU to LRU and LRU to external interface communication path faults.
Compliant	Compliant
Compliance Rationale	DDD Section 7.2.6 All SPS faults identified in the FMECA can be detected. There is no further analytical proof of compliance at this time.
L3-120	**SPS off-line memory and calculation fault detection** When commanded and with the SPS Administrative Modes set to OFFLINE, SPS shall detect and report the following faults: 1. Stuck or incorrect memory cells, whether a direct fault or manifested as such, **2.** Calculation faults that may lead to incorrect data products, whether a direct fault or manifested as such.
Compliant	Compliant
Compliance Rationale	DDD Section 6.9
L3-121	**SPS on-line built-in self-test capability** While the SPS Administrative Mode is set to ONLINE or MAINTENANCE, SPS shall perform diagnostic tests to detect and isolate LRU and sub-element faults.
Compliant	Compliant
Compliance Rationale	DDD Section 6.9
L3-122	**SPS on-line fault detection performance** While the SPS Administrative Mode is set to ONLINE or MAINTENANCE, SPS shall detect and report 99% of all Critical Failures. Note: A Critical Failure is a failure that would prevent the SPS of being "Operationally Capable".
Compliant	Compliant
Compliance Rationale	DDD Section 6.9 All SPS faults identified in the FMECA can be detected. There is no further analytical proof of compliance at this time.

L3-123	**SPS on-line fault isolation performance** While the SPS Administrative Mode is set to ONLINE or MAINTENANCE, the SPS shall isolate more than 95% of all failures down to an LRU level. Note: SPS maintainer implements part of the fault isolation capability by removing and replacing suspected LRUs to isolate the faulty LRU.
Compliant	Compliant
Compliance Rationale	DDD Section 10.3 All SPS faults identified in the FMECA can with maintainer help be isolated to one LRU. There is no further analytical proof of compliance at this time.
L3-124	**SPS on-line communications fault detection** While the SPS Administrative Mode is set to ONLINE or MAINTENANCE, SPS shall detect all utilised sub-element LRU to LRU and LRU to external LRU communication path faults with a detection probability of at least 99%.
Compliant	Compliant
Compliance Rationale	All SPS faults identified in the FMECA can be detected. There is no further analytical proof of compliance at this time.
L3-125	**SPS monitor and report operational state** SPS shall monitor its operational state and make available the information upon request in line with the software standard [RD2].
Compliant	Compliant
Compliance Rationale	DDD Section 3.2.3, 3.3, 5.2.1.1, 5.6.2
L3-126	**SPS in-system programmability** SPS programmable devices shall be in-system programmable in cases where the safety of personnel and equipment are not affected.
Compliant	Compliant
Compliance Rationale	Everything is compliant. Both the TPM and the RMB/SMB are in-system programmable. Actually, they must be as they are initially programmed after assembly. ISP is a last resort; all boards can be remotely upgradable. ISP occurs when for some reason the basic code that allows remote upgrade is corrupted. See DDD Section 6.6,
L3-127	**SPS software updates** SPS equipment shall facilitate major software updates within the LFAA maintenance time allocations. Note: Software maintenance down time (MDT) is defined as the time per year that LFAA is unavailable as result of a LFAA software defect repairs and general software maintenance activities during the telescope operational phase. It's assumed that all major LFAA software defects are removed during construction and the first year of warranty. LFAA software defect repairs and maintenance that don't require LFAA down-time are excluded from MDT.
Compliant	Compliant
Compliance Rationale	Software update is performed using LMC network, with very limited down time (DDD section 6.6). Code commissioning is described in DDD section 15.2
L3-128	**SPS maintenance provisions** SPS repairable items shall have maintenance provisions such as test points, accessibility, and plug-in components.
Compliant	Compliant
Compliance Rationale	SPS sub-element is expected to be compliant see DDD sections 5.4.1, 5.4.2, 5.4.3
L3-129	**SPS LRU removal**

	SPS LRUs shall be mounted such that removal of any single LRU does not require the removal of other LRUs.
Compliant	Compliant
Compliance Rationale	Compliant by design DDD section 5.4.4. See also the SKA SPS Cabinet Specification document [RD12]
L3-130	**SPS mounting preclusion** SPS shall include provisions to preclude incorrect assembly to eliminate the possibility of equipment damage or mis-operation.
Compliant	Compliant
Compliance Rationale	Compliant by design. DDD Section 5.4.4
L3-131	**SPS stand-offs and handles** SPS shall provide equipment handles and stand-offs to facilitate the installation and handling and to mitigate damage of the equipment during out-of-system repair.
Compliant	Non-compliant
Compliance Rationale	It is expected that the design will be compliant, but this isn't documented in the DDD yet
L3-132	**SPS mounting guides** Where applicable, SPS shall provide mounting guides and location pins on equipment to facilitate maintenance.
Compliant	Compliant
Compliance Rationale	The TMPs uses card guides to mechanically guide the installation of LRUs into the sub-rack. All other chassis-based equipment (e.g., switches) are mechanically supported on slide rails to facilitate installation and removal.
L3-133	**SPS module labelling** SPS labelling of modules shall be in a conspicuous location, such that it is readable when the module is removed or installed in its intended operating environment, when such labelling doesn't impede functionality and/or performance.
Compliant	Compliant
Compliance Rationale	By design SPS equipment has conspicuous labelling visible when removed or installed.
L3-134	**SPS Storage of Equipment** SPS equipment, while in its storage packaging, shall withstand, and shall operate to specification as defined herein after exposure to, the storage environmental conditions as defined in “Class 1.1: Weather protected, partly temperature-controlled storage locations” of the ETSI EN 300 019-1-1 standard and defined in BS EN IEC 60721-3-1. 1. Climatic Conditions 1K3 2. Biological Conditions 1B2 3. Chemical conditions 1C2 4. Dust and Sand conditions 1S2 **5.** Shock & Vibration Conditions 1M2
Compliant	Compliant

Compliance Rationale	DDD Section 12.2, 12.4: equipment whilst in storage shall withstand conditions defined by Class 1.1, and still be operational when required for operations.
L3-135	**SPS Transportation Environment** All components and spares of the SPS, in their transport packaging, shall be safe from damage while, and shall perform to specification as defined herein, after being transported under conditions as defined in "Class 2.2: careful transportation" of the ETSI EN 300 019-1-2 standard [RD36] and defined in BS EN IEC 60721-3-2: - Climatic conditions 2K5H - Biological conditions 2B3 - Chemical conditions 2C1 - Dust and Sand conditions 2S3 - Shock & Vibration conditions 2M3
Compliant	Compliant
Compliance Rationale	Environmental - Section 12.3.1 - SPS transports equipment for construction and maintenance in protected environmental packaging which complies to Class 2.2.
L3-136	**SPS COTS operating environment** The SPS "off-the-shelf" equipment shall perform to specification as defined herein during operation under the environmental conditions as defined in the ETSI EN 300 019-1-3 standard for "Class 3.6: Telecommunication control room locations" or equivalent.
Compliant	Compliant
Compliance Rationale	Environmental - DDD Section 12.3, 12.3.2, 12.3.3, 12.4 - SPS equipment operates in conditions defined by Class 3.1.
L3-137	**SPS Seismic Resilience** SPS racks and equipment shall survive and be fully operational after seismic events resulting in a maximum peak ground acceleration of 1 m/s^2. Note: Seismic events include underground collapses in addition to earthquakes.
Compliant	Compliant
Compliance Rationale	Implementation - DDD Section 12.3.1 - SPS racks are mechanical fastened to the floor and each other within the CPF and RPFs. The centre of gravity is also positioned below the centre of the rack to provide added mechanical stability.
L3-138	**SPS serial and part numbers** SPS equipment items identified in the SKA Logistics Analysis and Configuration Item Plan as needing individual characterisation shall be marked with a label displaying a unique Serial Number and Part Number. The label should normally be in an easily visible location but may also include embedded identification for items such as embedded firmware/software.
Compliant	Compliant
Compliance Rationale	DDD Section 16.6.1, 16.7
L3-139	**SPS marking method** Where items used in SPS require labelling, the method of marking shall be compliant with the SKA Logistic Analysis Plan. The nature of the item, its

	environment and its use will determine the method. Where items used in SPS require labelling, the method of marking shall be compliant with the SKA Logistic Analysis Plan. The nature of the item, its environment and its use will determine the method.
Compliant	Compliant
Compliance Rationale	DDD Section 16.6.1
L3-140	**SPS electronically readable or scannable ID** Items used within the SPS shall be marked with a unique Electronically readable or scannable ID, in accordance with the SKA Logistic Analysis Plan and Configuration Plan. The ID may be serial number or part number or both or in some cases this may not be needed.
Compliant	Compliant
Compliance Rationale	DDD Section 16.6.1
L3-141	**SPS package marking** All packaging of items used in SPS shall be marked to uniquely identify the contents in accordance with the SKA Logistics Analysis Plan. The identification is by part number and serial number.
Compliant	Compliant
Compliance Rationale	DDD Section 16.6.1
L3-142	**SPS cable identification** Each SPS cable end shall carry an identifier that uniquely defines the connector it needs to connect to.
Compliant	Compliant
Compliance Rationale	DDD Section 16.6.1
L3-143	**SPS connector plate identification** All SPS connector plates shall carry identification labels for connectors.
Compliant	Compliant
Compliance Rationale	By design SPS connector plates have identification labels for each connector.
L3-144	**SPS user access control** SPS shall provide hardware and communication access to any authenticated user. Note: this means that user authentication for access to SPS is provided by MCCS with TM owning the user database.
Compliant	Compliant
Compliance Rationale	SPS access and control is based on authorised users/roles, as per EN 50600-2-5, Data centre facilities and infrastructures, Part 2-5, Security systems.

Table 17-1 Compliance Matrix

18 Appendix List of TBD TBCs

This section contains a summary of all TBDs (Table 18-1) and TBCs (Table 18-2) in the DDD. These tables do not include TBDs and TBCs in the L3 requirements or in any of the applicable ICDs. Details on these TBDs and TBCs can be found in the LFAA.SPS Requirements Specification [AD32] and the applicable interface documents [AD34].

ID	Section	Description	Resolution Plan
TBD1	4.1	Access and authentication responsibility	This is a system issue that needs to be resolved within the SKAO. However, there has been consideration given to security aspects of the implementation already.
TBD2	4.1	Interface TBDs	Further work at system level is required to complete and refine ICDs
TBD3	5.4.3.3	Bit and Packet errors	Associated with the LFAA to CSP interface, further work at system level is required to quantify the acceptable packet errors in relation to overall Telescope performance
TBD4	5.6.2.2	Sub-rack management board communication protocols	Further work is required as part of Bridging and Design Adoption to identify the protocols used to communicate to the Subrack management board.
TBD5	5.6.2.4	Cabinet monitoring low level interface protocols	As part of Bridging and Design adoption, the protocols associated with control and monitoring of low-level items such as cooling devices. Typically, this would be I^2C or equivalent.
TBD6	9.5.3	Battery size	Further design analysis, as part of Bridging is required to determine the size of battery that the “new power manager” needs to manage

Table 18-1 Table of TBDs

ID	Section	Description	Resolution Plan
TBC1	9.5.3	Unsequenced switch shutdown	As part of prototyping in Bridging, it should be confirmed that switches can have an unsequenced power down. This should also include investigation of power down mid firmware update.

Table 18-2 Table of TBCs

19 Appendix Intellectual Property Declaration

19.1 Organisation

The following pages provide the Intellectual Property declaration from Sanitas:

SKA Intellectual Property Rights (IPR) Notification Form

Please indicate your response to the listed requirements

Please use one form for each IPR you wish to notify

No	Requirement	Response
1	Description of technology or work in relation to which IPR is said to exist. *(Use continuation sheets if necessary.)* *(This should include a brief description of what the function of the technology is and of how such technology carries out that function.)*	Ethernet management and test interface, including Xilinx SMAP test interface. This IP allow the management, test and quality assurance of FPGA based complex design
2	Brief outline of the relevance of this technology or work for the SKA Project. *(Use continuation sheets if necessary.)* *(This should include the identification of the products in which the technology or work is used – reference to an item in the approved Product Breakdown Structure is required here)*	This IP allow to efficiently manage the large number of TPM remote FPGA base system and to estimate the contribute to the MTBF of the FPGA design

SKA Intellectual Property Rights (IPR) Notification Form

3	Details of any filings for patents, utility models, registered designs etc. made in respect of the technology or work. *(This should include the application number of the right, any publication number and the number of any granted right.)*	Patented, not renewed, in 2010
4	Date on which first filings for patents, utility models, registered designs etc. in respect of the technology or work were made.	About 2006, request for patent date
5	Location of patent/design or trade mark office in which first filing(s) for the IPR was/were made. *(This will be a national or international trade mark, patent or registered design office such as the EPO, OHIM, USPTO or a national office (e.g. the German national patent office).)*	Italy
6	Countries/Jurisdictions for which patent, utility model, registered design etc. protection is or has been sought.	Italy

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7	Type of IPR. *(State whether patent, copyright, design right, registered design, utility model, design patent, semiconductor topography right, database right, confidentiality rights or rights in trademarks or other rights.)*	☐ Patent ☐ Copyright ☒ Design Rights ☐ Registered Design ☐ Utility Model ('Innovation patent') ☐ Design Patent ☐ Semiconductor topography rights ☐ Database rights ☐ Confidentiality rights (Trade Secrets) ☐ Trademarks ☐ Other rights
8	Date of creation of the technology or work in which the IPR is said to exist.	2006 and 2010 for ethernet extension
9	Date on which IPR is said to have come into effect and become enforceable. *(This will either be the date of grant for a registered IPR or the date of creation of a physical embodiment of the work in relation an unregistered IPR.)*	Design start
10	Date on which IPR is said to cease to have effect and become no longer enforceable.	Design and production ended
11	Is the IPR said to be Background IPR or Foreground IPR? *(These are as defined in the IP Policy)*	☒ Background IPR ☐ Foreground IPR ☐ N/A (Third Party IPR)
12	If the IPR is said to be Background IPR but was created after you became an SKA Contributor then please provide a brief explanation as to how it came to be created outside the SKA Project.	Created before

SKA Intellectual Property Rights (IPR) Notification Form

13	Countries/jurisdictions in which IPR is said to have effect.	All
14	Identify any key requirements as to territory, exclusivity, field of use and exclusions from field of use, duration, necessary business relationships, etc., that you would likely seek to impose on any prospective licensee (including the SKAO). *(Please ensure that any terms that are to be imposed on the use of the IP in the SKA appear here explicitly.)*	na
15	Details of individual creators of the technology or work in relation to which IPR is said to exist. *(State the names and addresses of all those persons said to have created the technology or work. List no more than five persons.)*	Sanitas EG employee, Monica Alderighi Sergio d'angelo

SKA Intellectual Property Rights (IPR) Notification Form

16	Name of IPR owner.	Sanitas EG srl
17	Postal Address of IPR owner.	Viale Restelli 3, 20124, Milano (IT)
18	Contact Details for IPR owner. *(State the name, email address and telephone number of the contact person.)*	Sandro Pastore, sandro.pastore@sanitaseg.it, cell +39 320 0945069

19	Details of any licences of the IPR already granted to third parties. *(State the name of licensee, licensed activity, date and term of licence for the IPR being registered here.)*	Name of licensee: na Licensed application: na Date of commencement: na Term of licence: na
20	Deleted	
21	Details of any licences that are likely to be granted to third parties in respect of the IPR in the future. *(State the name of prospective licensee, licensed activity, likely date and term of licence.)*	Name of prospective licensee: na Licensed application: na Likely date of commencement: na Term of licence: na

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SKA Intellectual Property Rights (IPR) Notification Form

22	Status of embodied IPR ('Third Party IPR') Permissions. *(State details of any known IPR not owned by you which use of this technology or work would be likely to infringe absent an appropriate licence. Details to include nature of the embodied IPR and details of the owner of that IPR together with details of any approaches made to the owner to obtain any necessary licence(s).)*	na
23	Author Record. *(State the name and job title of the person who created the record.)*	Sandro Pastore, Sanitas EG, CEO
24	Date of Record. *(State the date that this record was last updated.)*	23 November 2017
25	Signature.	